IC/semiconductors

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High mobility/high K 3D x3D   MEMORY

PPACR (performance, power, area, cost reliability)

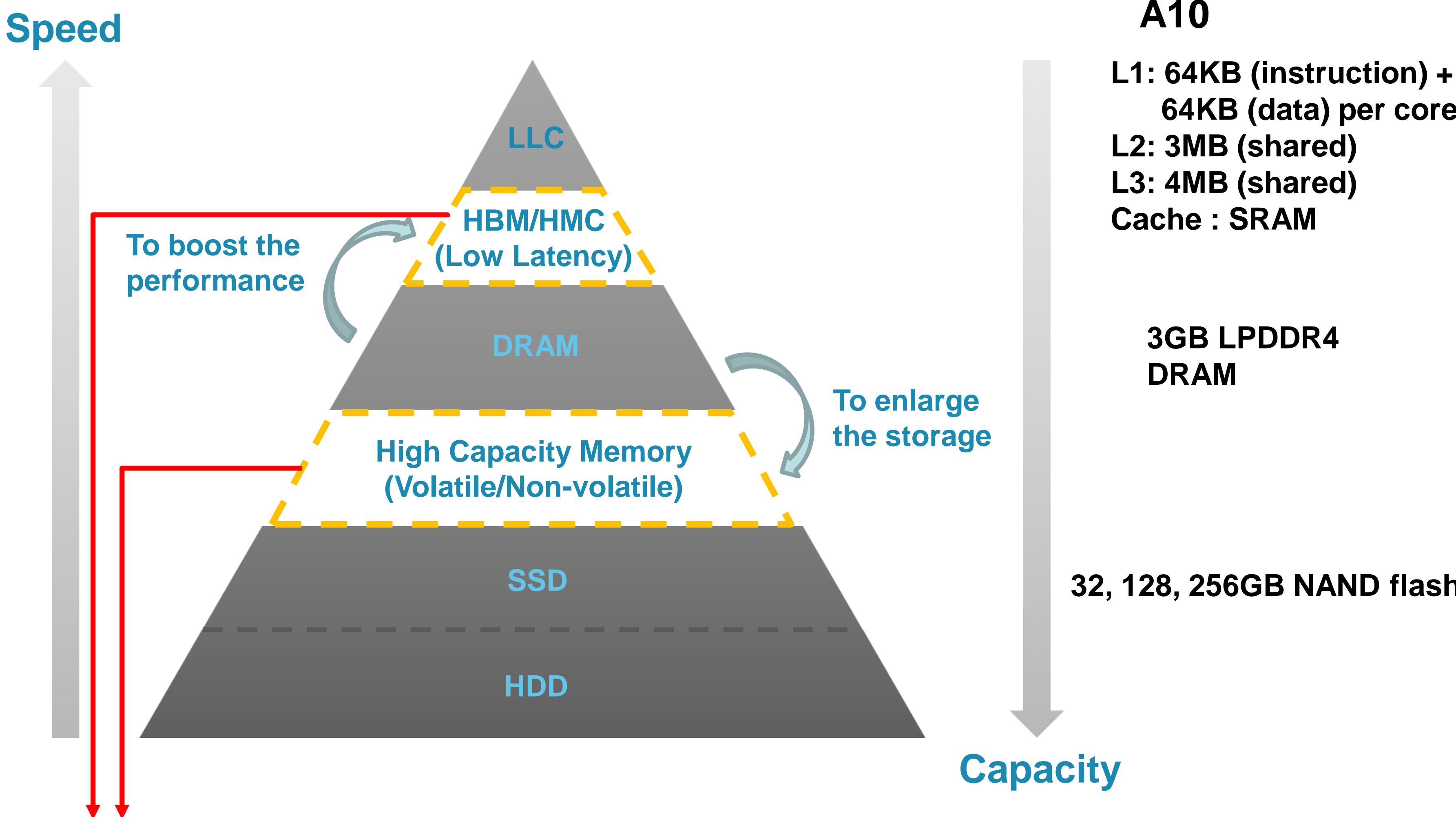
學未來，需要再學歷史

- 學生：物理好，數學好，化學好
  實驗好(人緣好, 黑手)

- 工程師：team work/meet deadline

- 管理：vision (IEDM/VLSI papers)

Memory Hierarchy iPhone 7 plus



Gaps hopefully filled by MRAM

http://www.fansdeapple.com/showthread.php?t=91513

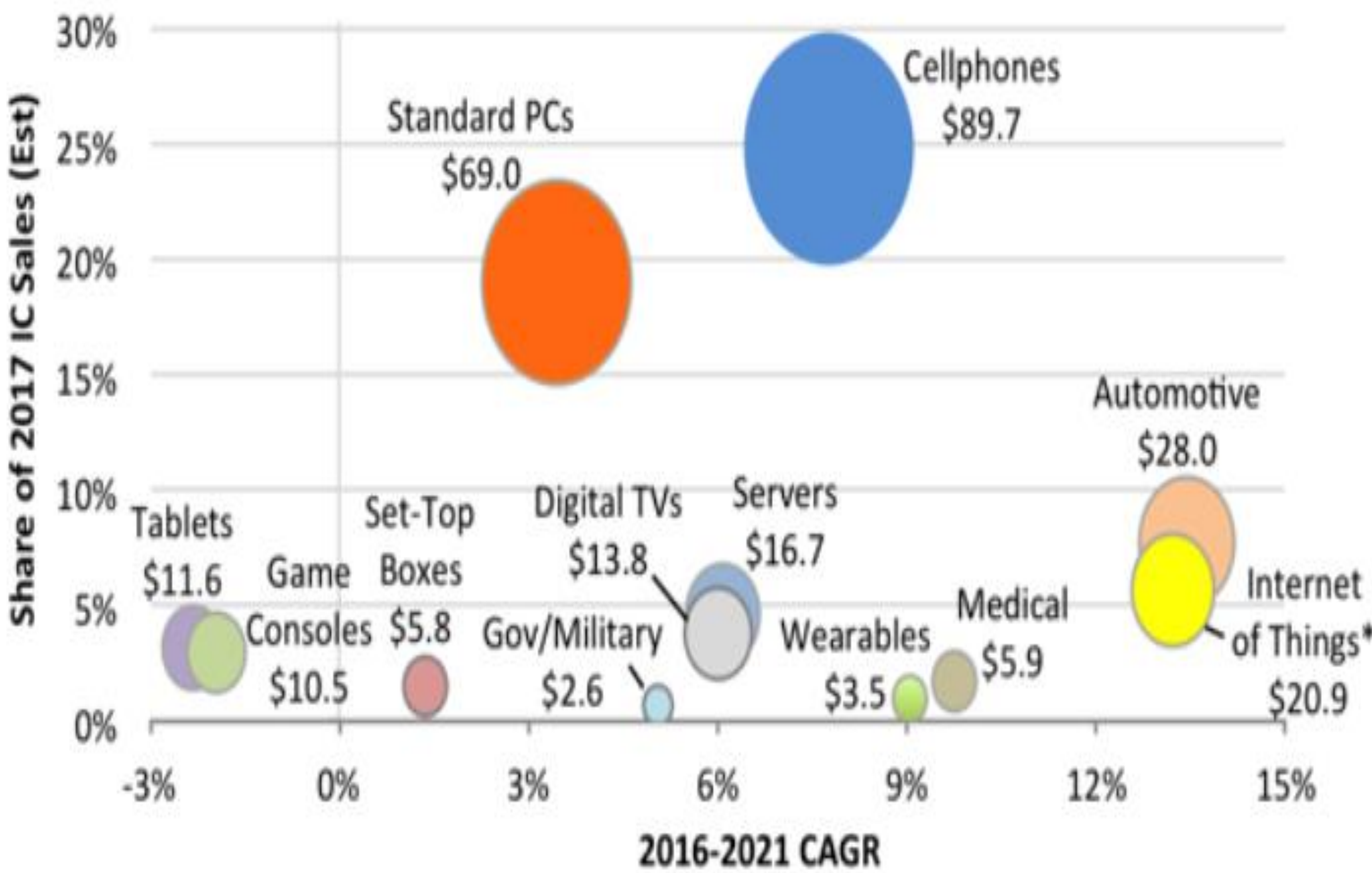
Future:
AI, Big Data, Connectivity/Cloud= IC/Semiconductor

Science vs Technology

Internet of things 50B devices	x	Big Data 35 Zetta bytes	=	Revenue growth Cost saving Margin gain

- **Collection by Sensors: optical/MEMS/N-x node**
- **Connectivity : Wireless 5G (IOT + 4G/WiFi +mm Wave) +**
- **Cloud : compute (Intel/IBM) Memory (Samsung)**

This slide will be shown in the presentation



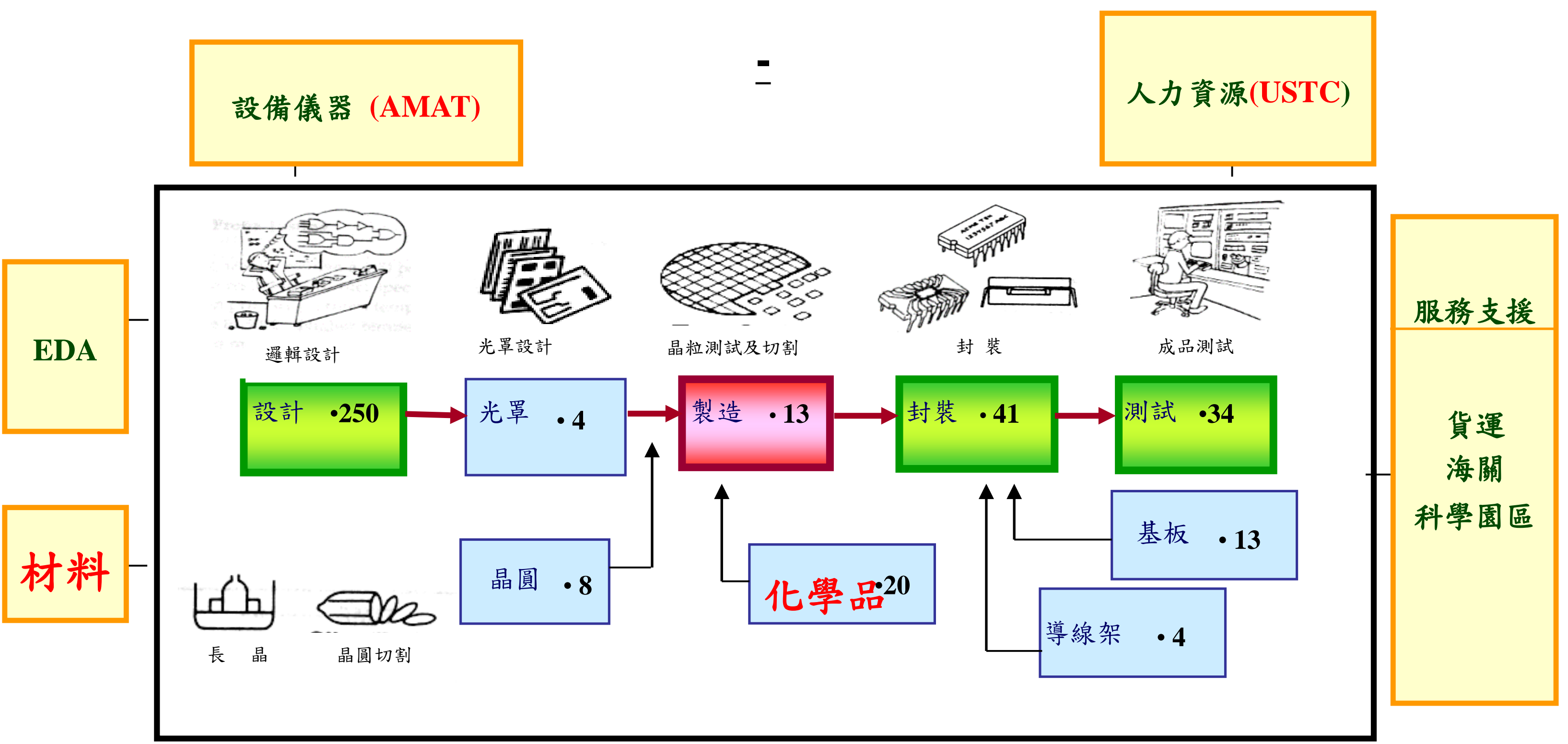
*Covers only the Internet connection portion of systems.

2018 Top 16 Semiconductor Sales Leaders

2018 Rank	2017 Rank	Company	Headquarters	2017 Total Semi Sales ($ M)	2017 Total Semi Sales ($M)	2018/2017 Growth (%)
1	1	Samsung	South Korea	65,882	83,258	26%
2	2	Intel	U.S.	61,720	70,154	14%
3	4	SK Hynix	South Korea	26,722	37,731	41%
4	3	TSMC	Taiwan	32,163	34,209	6%
5	5	Micron	U.S.	23,920	31,806	33%
6	6	Broadcom Ltd	U.S.	17,795	18,455	4%
7	7	Qualcomm	U.S.	17,029	16,481	-3%
8	9	Toshiba/Toshiba memory	Japan	13,333	15,407	16%
9	8	TI	U.S.	13,910	14,962	8%
10	10	Nvidia	U.S.	9,402	12,896	37%
11	12	ST	Europe	8,313	9,639	16%
12	15	WD/SanDisk	U.S.	7,840	9,480	21%
13	11	NXP	Europe	9,256	9,394	1%
14	13	Infineon	Europe	8,126	9,246	14%
15	14	Sony	Japan	7,891	8,042	2%
16		MTK	Taiwan	7,821	7,900	1%

Source: IC Insights

半導體產業結構



1.上下游產業鏈完整
2.專業分工配合度高
3.產業群聚效果顯著
4.週邊支援產業完善

資料來源：工研院IEK(2004/03)

We need young talents

Moore's Law (scaled FETs)

- Intel co-founder Gorden Moore noticed in 1964
- Transistor density on a chip doubles per generation (2x/generation)
- Amazingly still correct, likely to keep until 20xx

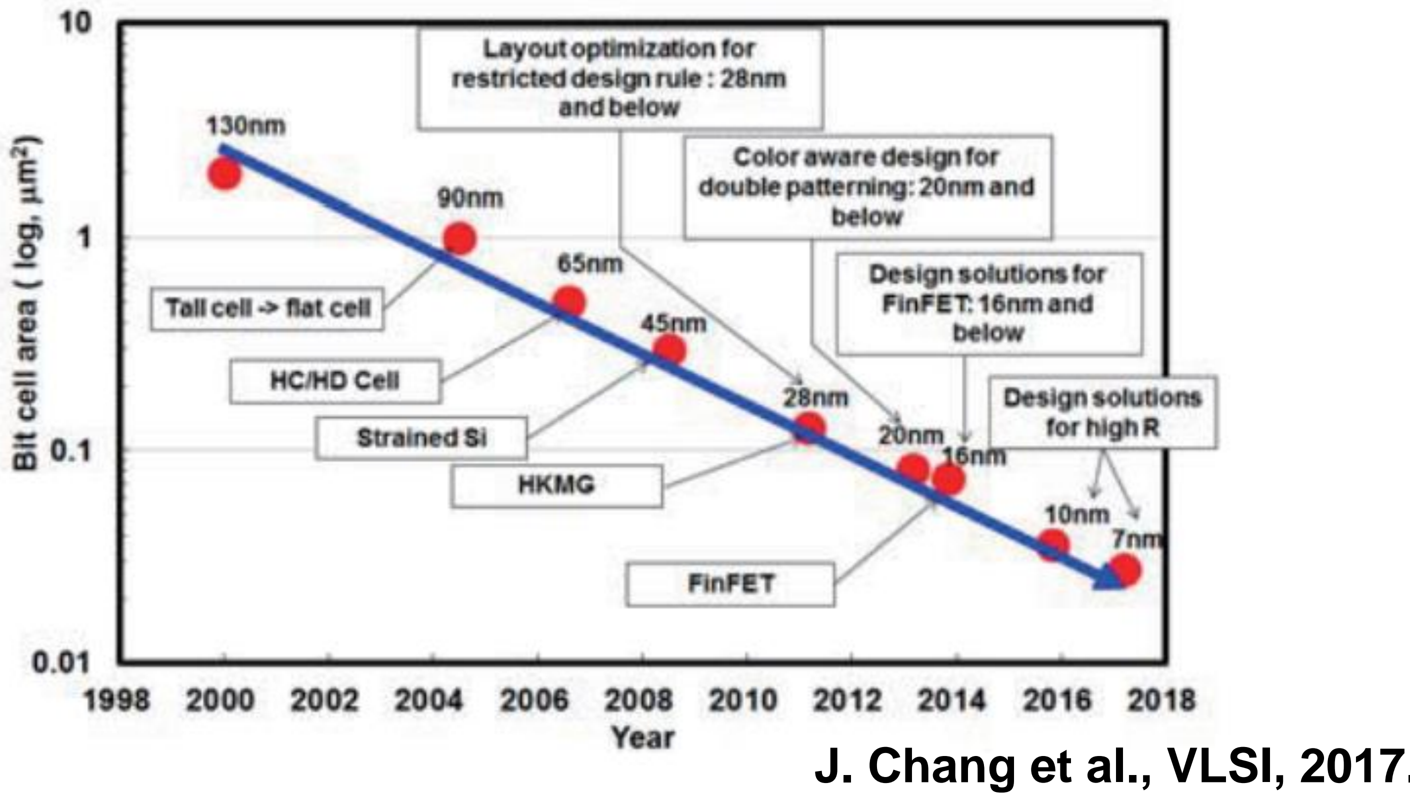
MORE Than MOORE: **Sensor/MEMS, Analog, RF, …**

How to do this

- Must: Device footprint (next generation) =L (current generation) x 0.7
- (optional) Chip area = 2x

Road Map Semiconductor Industry
45 32 22/20 16/14

	1995	1997	1999	2001	2004	2007
Minimum feature size	**0.35**	**0.25**	**0.18**	**0.13**	**0.09**	**0.065**
DRAM Bits/chip Cost/bits @ volume (millicents)	 64 M 0.017	 256 M 0.007	 1 G 0.003	 4 G 0.001	 16 G 0.0005	 64 G 0.0002
Microprocessor Transistors/cm^2 Cost/Transistor @ volume (millicents)	 4 M 1	 7 M 0.5	 13 M 0.2	 25 M 0.1	 50 M 0.05	 90 M 0.02
ASIC Transistors/cm^2 Cost/Transistor @ volume (millicents)	 2 M 0.3	 4 M 0.1	 7 M 0.05	 13 M 0.03	 25 M 0.02	 40 M 0.01
Wafer size (mm)	200	200	200 - 300	300	300	300



J. Chang et al., VLSI, 2017.

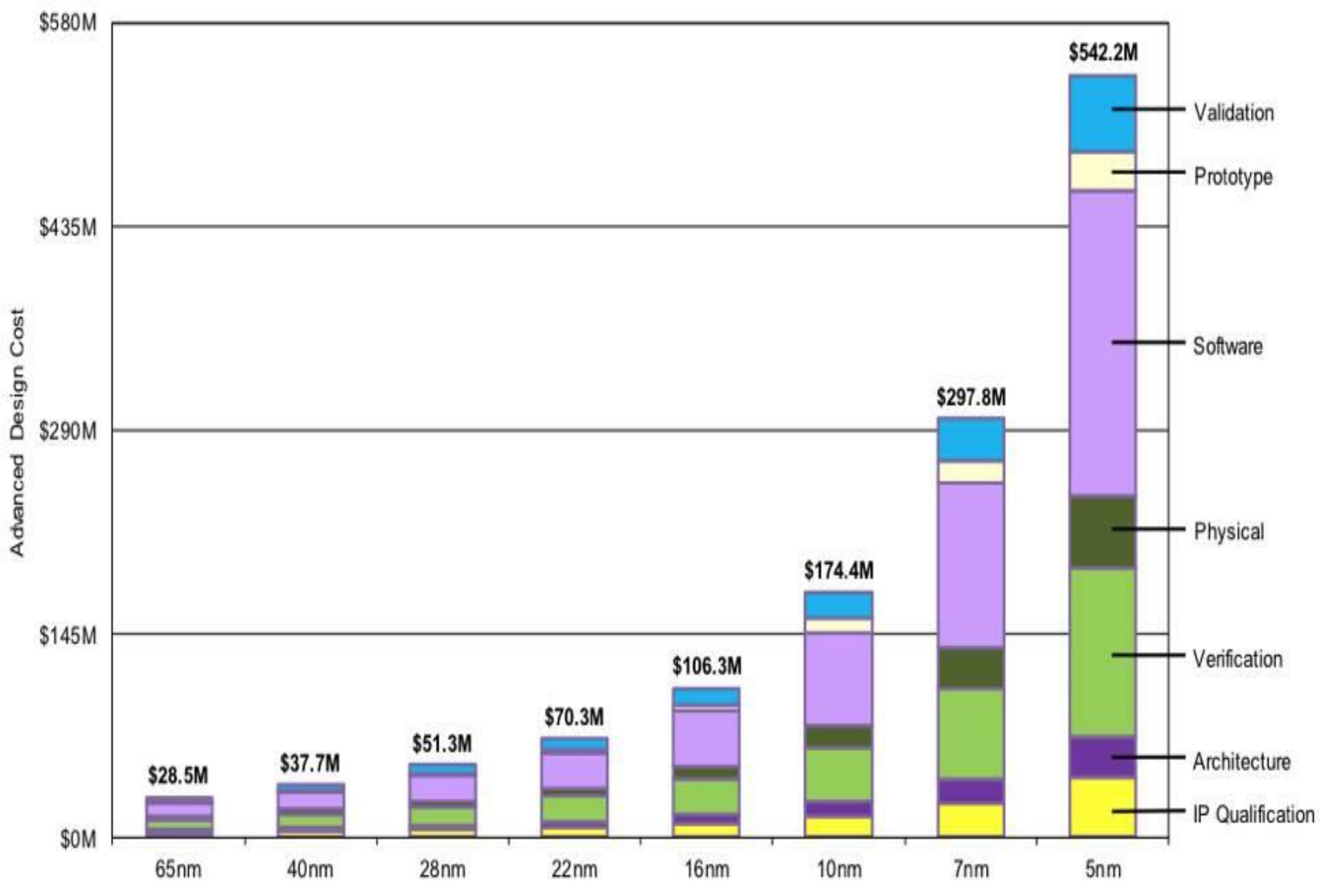
- **SRAM 6T bit-cell area scaling trends from 0.13um to 7nm technolo**
- **What does 7 nm node mean?**

Technology Portfolio

● → Available
○ → In Development

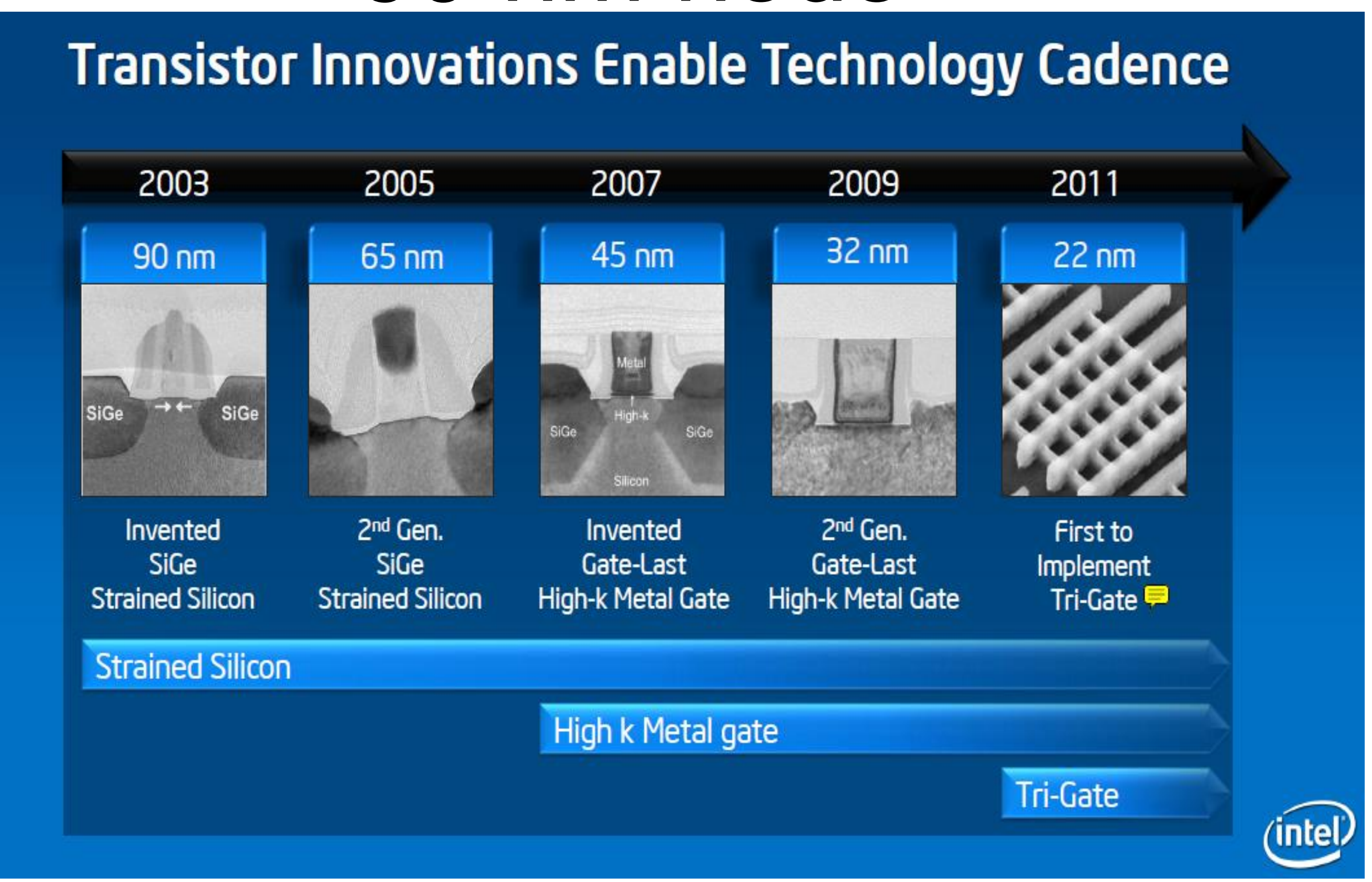
	MEMS	Image Sensor	Embedded NVM	RF	Logic	Analog	High Voltage	Embedded DRAM	BCD-Power IC
5 nm					○				
7 nm					●				
10 nm					●				
16/12 nm				●	●	○			
20 nm					●	●			
22 nm			○	○	○	○			
28 nm		○	○	●	●	●	○		
40 nm		●	●	●	●	●	●	●	○
65/55 nm		●	●	●	●	●	●	●	
90/80 nm		●	●	●	●		●	●	○
0.13/0.11 μm	○	●		●	●	●	●		●
0.18/0.15 μm	●	●	●	●	●	●	●		●
0.25 μm	●	●	●	●	●	●	●		●
0.35 μm	●	●	●	●	●	●	●		●
>0.5 μm	●	●	●	●	●	●	●		●

- **3/2 nm technology node**
- **DRAM and FLASH**

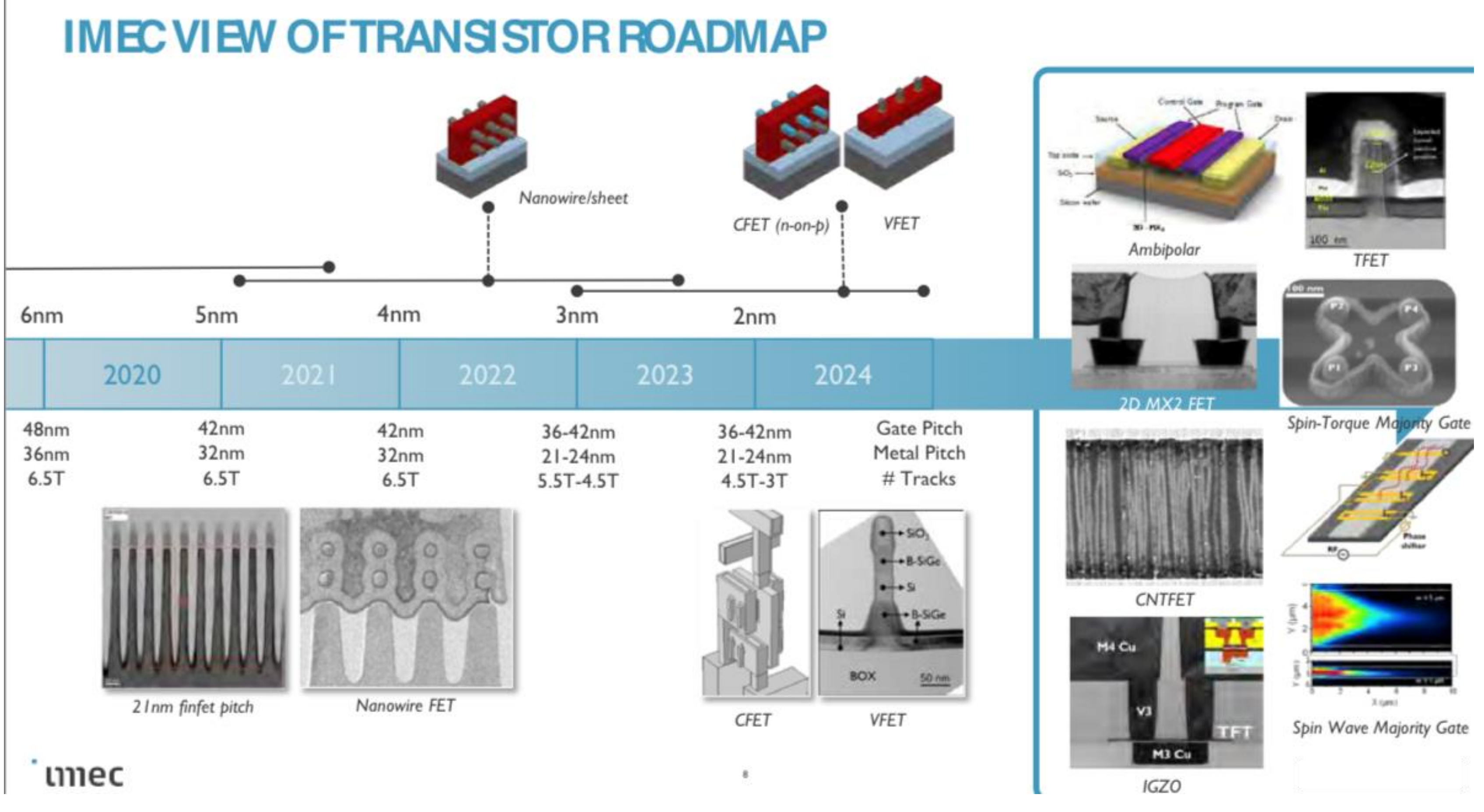


Design cost only, not include manufacturing

Strained Si starting from 90 nm node



- Enabling technologies: high mobility, high-k/metal gate, 3D transistor


IMEC VIEW OF TRANSISTOR ROADMAP
Nanowire/sheet
CFET (n-on-p)
VFET
6nm
5nm
4nm
3nm
2nm
2020
2021
2022
2023
2024
48nm
36nm
6.5T
42nm
32nm
6.5T
42nm
32nm
6.5T
36-42nm
21-24nm
5.5T-4.5T
36-42nm
21-24nm
4.5T-3T
Gate Pitch
Metal Pitch
Tracks
21nm finfet pitch
Nanowire FET
CFET
VFET
BOX
Ambipolar
TFET
2D MX2 FET
Spin-Torque Majority Gate
CNTFET
IGZO
M4 Cu
V3
M3 Cu
TFT
Spin Wave Majority Gate
imec

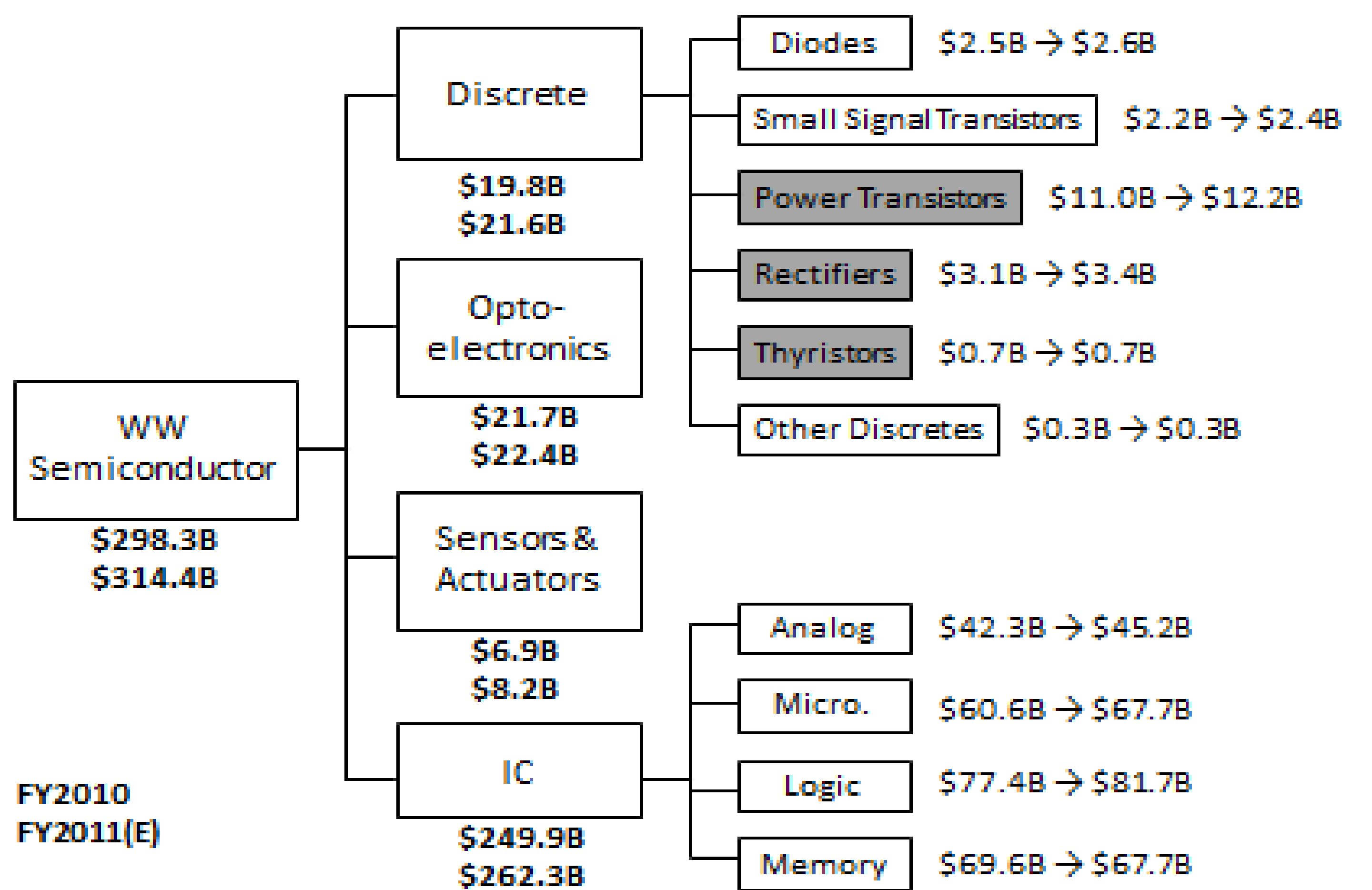
How far can we go?

Table 2: Device roadmap enabling More Moore scaling: 1) Device architecture, 2) Device module characteristics, 3) Performance boosters.

YEAR OF PRODUCTION	2015	2017	2019	2021	2024	2027	2030
Logic device technology naming	P70M56	P54M36	P42M24	P32M20	P24M12G1	P24M12G2	P24M12G3
Logic industry "Node Range" Labeling (nm)	"16/14"	"11/10"	"8/7"	"6/5"	"4/3"	"3/2.5"	"2/1.5"
Logic device structure options	finFET FDSOI	finFET FDSOI	finFET LGAA	finFET LGAA VGAA	VGAA, M3D	VGAA, M3D	VGAA, M3D
	FinFET / FDSOI	FinFET / FDSOI	Lateral Nanowire / FinFET	Vertical Nanowire / Lateral Nanowire	Vertical Nanowire / Monolithic 3D	Vertical Nanowire / Monolithic 3D	Vertical Nanowire / Monolithic 3D
DEVICE ARCHITECTURE & MODULES							
Starting substrate	Si, SOI	Si, SOI	Si,SOI, SRB, QW	Si,SOI, SRB, QW	Si,SOI, SRB, QW	Si,SOI, SRB, QW	Si,SOI, SRB, QW
N-channel	Si	s Si	s Si, Ge	s Si, s Ge, IIIV	s Si, s Ge, IIIV	s Si, s Ge, IIIV	s Si, s Ge, IIIV
P-channel	Si	Si,SiGe	Si,SiGe	Si,SiGe	Ge	Ge	Ge
Channel formation	Etch	Etch, EPI	Etch, EPI	Etch, EPI	Etch, EPI	Etch, EPI	Etch, EPI
Contact material	Silicide	Low-SBH	Low-SBH	Low-SBH	Low-SBH	Low-SBH	Low-SBH
Contact integration	EPI	EPI	EPI WAC	WAC	WAC	WAC	WAC
DEVICE PERFORMANCE BOOSTERS							
Main performance booster	SCE finHeight Vt	SCE finHeight Vt	Parasitics finHeight	Parasitics finHeight	Low Vdd 3D	Low Vdd 3D	Low Vdd 3D
Scaling focus	Perf	Power	Power	Power	Function	Function	Function
Channel strain	Yes	Yes	Yes	Yes	Yes	Yes	Yes
S/D strain	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Transport scheme	DD	Quasi Ballistic	Quasi Ballistic	Ballistic	Ballistic TFET, JFET, NCMOS	Ballistic TFET, JFET, NCMOS	Ballistic TFET, JFET, NCMOS, Spin

Acronyms used in the table (in order of appearance): FDSOI: Fully-Depleted Silicon-On-Insulator (FDSOI), LGAA: Lateral Gate-All-Around-Device (GAA), VGAA: Vertical GAA, M3D: Monolithic-3D, SRB: Strain-Relaxation-Buffer, QW: Quantum well, SBH: Schottky Barrier Height, WAC: Wrap-around-contact, DD: Drift-diffusion, TFET: Tunneling FET, JFET: Junctionless FET, NCMOS: Negative-capacitance MOSFET.

IC/Semiconductor



2016年全球半導體元件市場

全球市場：338.9B美元

- Sensor: 9.1, 2.7%
- Discrete: 18.7, 5.6%
- Opto: 35, 10.4% ：CIS, Si photonics
- IC:

  Analog, 46.5, 13.8%

  Memory, 72.4, 21.5% DRAM/FLASH

  Micro, 62.5, 18.6%

  Logic, 92.1, 27.4%

Fab Equipping Spending over Time
US $ Billion
(All Front End facilities. Including new, used, and in-house)
$70.00
$60.00
$50.00
$40.00
$30.00
$20.00
$10.00
$0.00
$29
$28
$34
$39
$26
$15
$35
$40
$34
$31
$37
$36
$40
$57
$63
2004
2005
2006
2007
2008
2009
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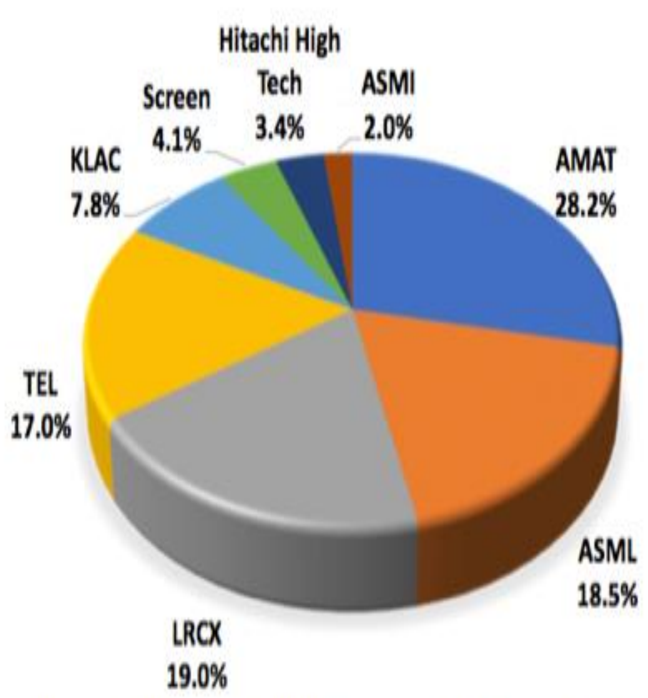
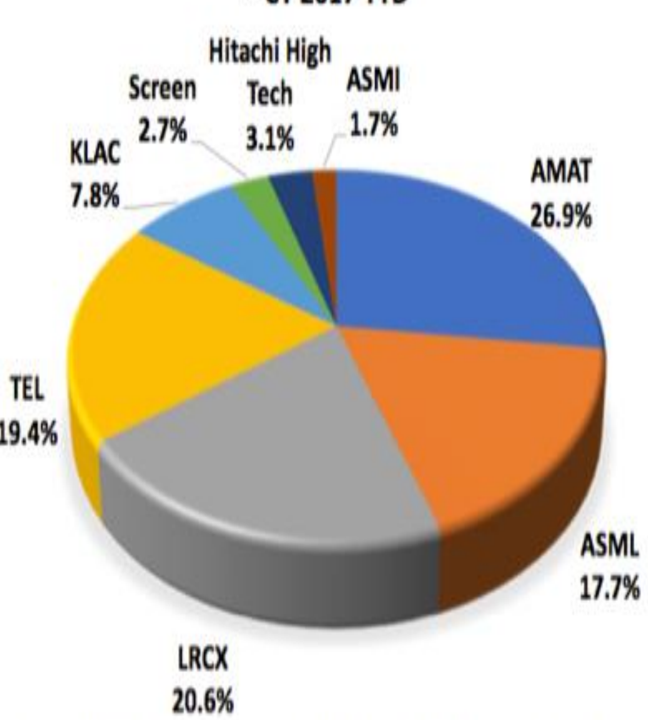
2015
2016
2017
2018
World Fab Forecast reports (Dec 4, 2017) published by SEMI

Semiconductor Equipment Shares
2016-2017 YTD



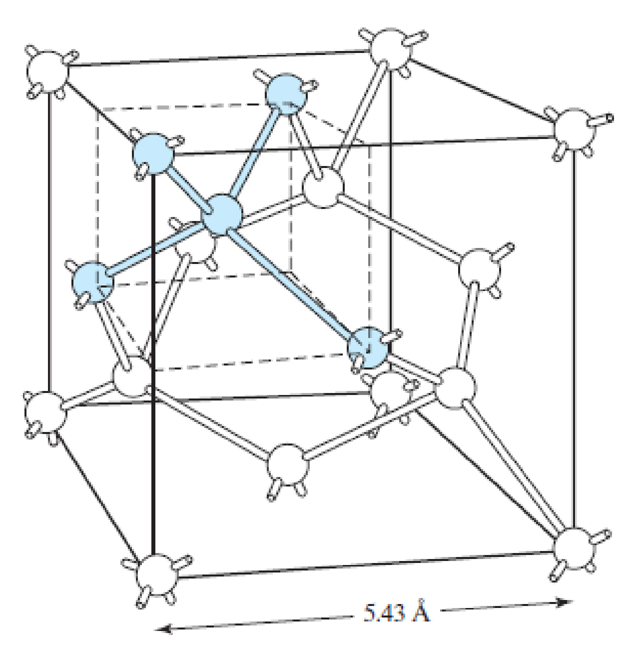


Silicon Crystal Structure (Ge, SiGe, GeSn)

- ***Unit cell*** of silicon crystal is cubic.

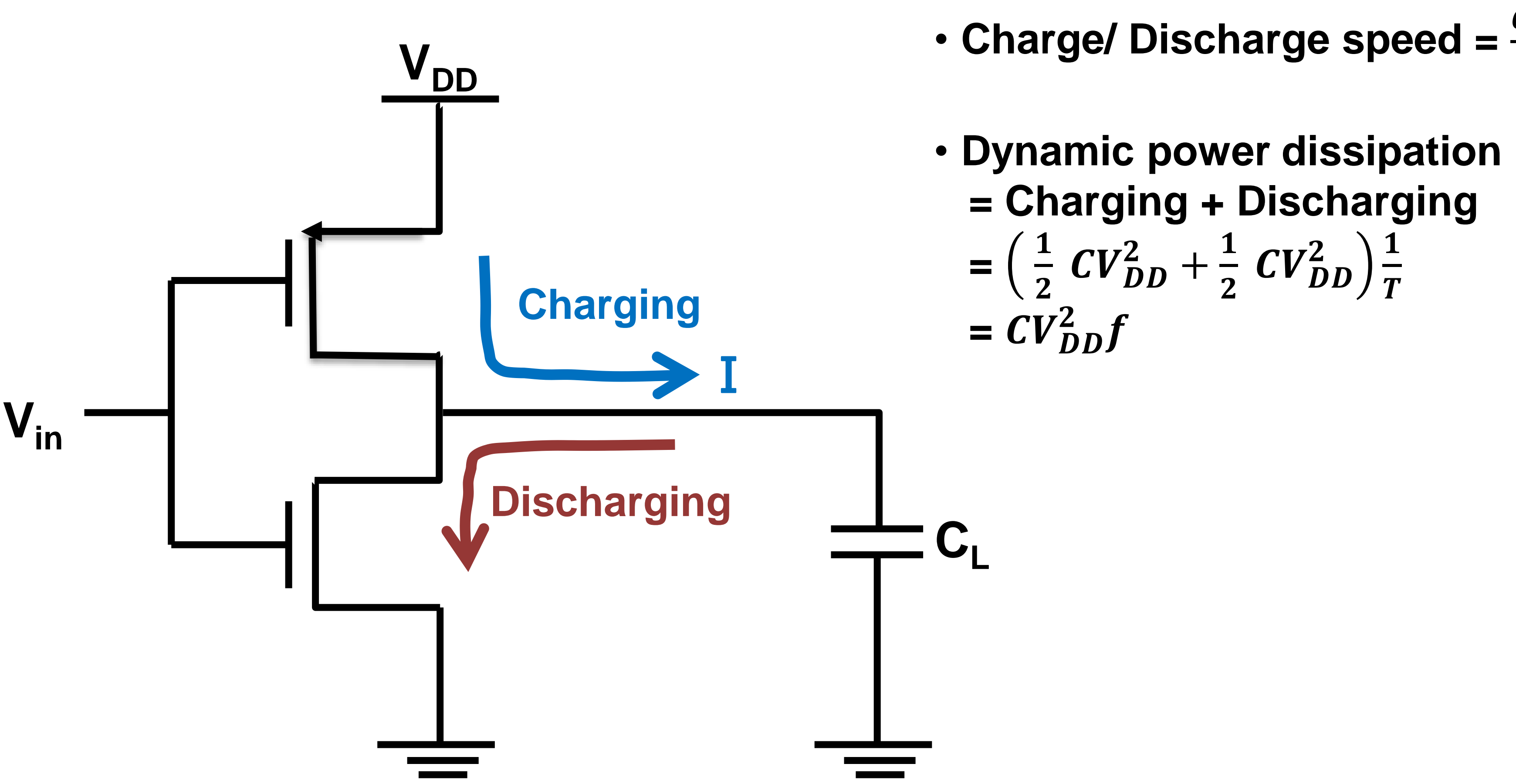
- ***Each Si atom has 4 nearest neighbors*.**

- **Si sp3**
- **Conduction band is ?**
- **Valence band is ?**



EE: Large I_{on} and small V_{dd}

- 要馬兒好又要馬兒不吃草



- Charge/ Discharge speed = $\frac{CV}{I}$
- Dynamic power dissipation
  = Charging + Discharging
  = $\left(\frac{1}{2}\,CV_{DD}^{2} + \frac{1}{2}\,CV_{DD}^{2}\right)\frac{1}{T}$
  = $CV_{DD}^{2}f$

Inverter → Ring oscillator

$$I_{on} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_t)^2$$

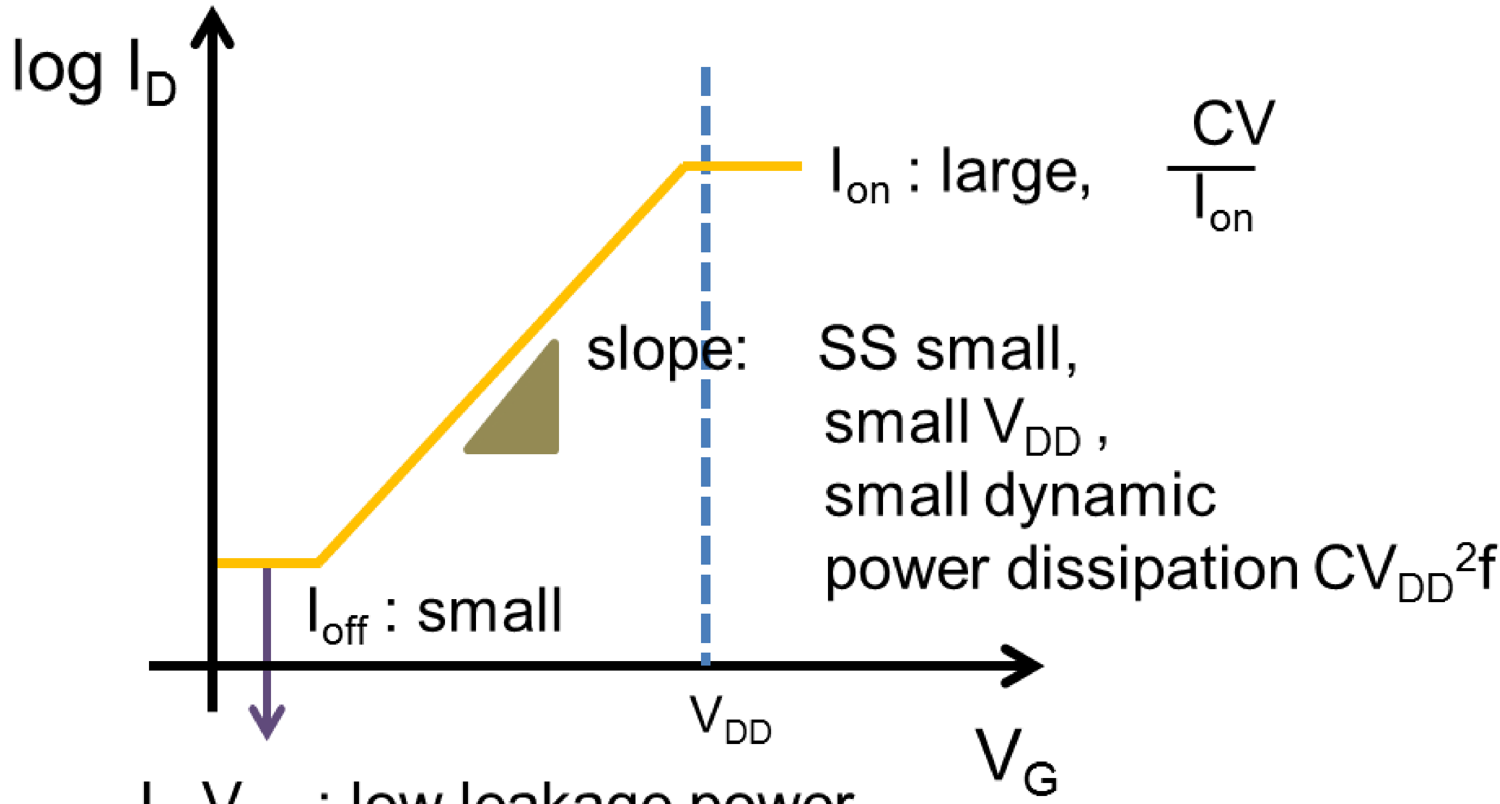
Large Ion → high speed CV/I

large μ_n , $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ → large ϵ_{ox} small tox→ large tunneling current (big Ig)

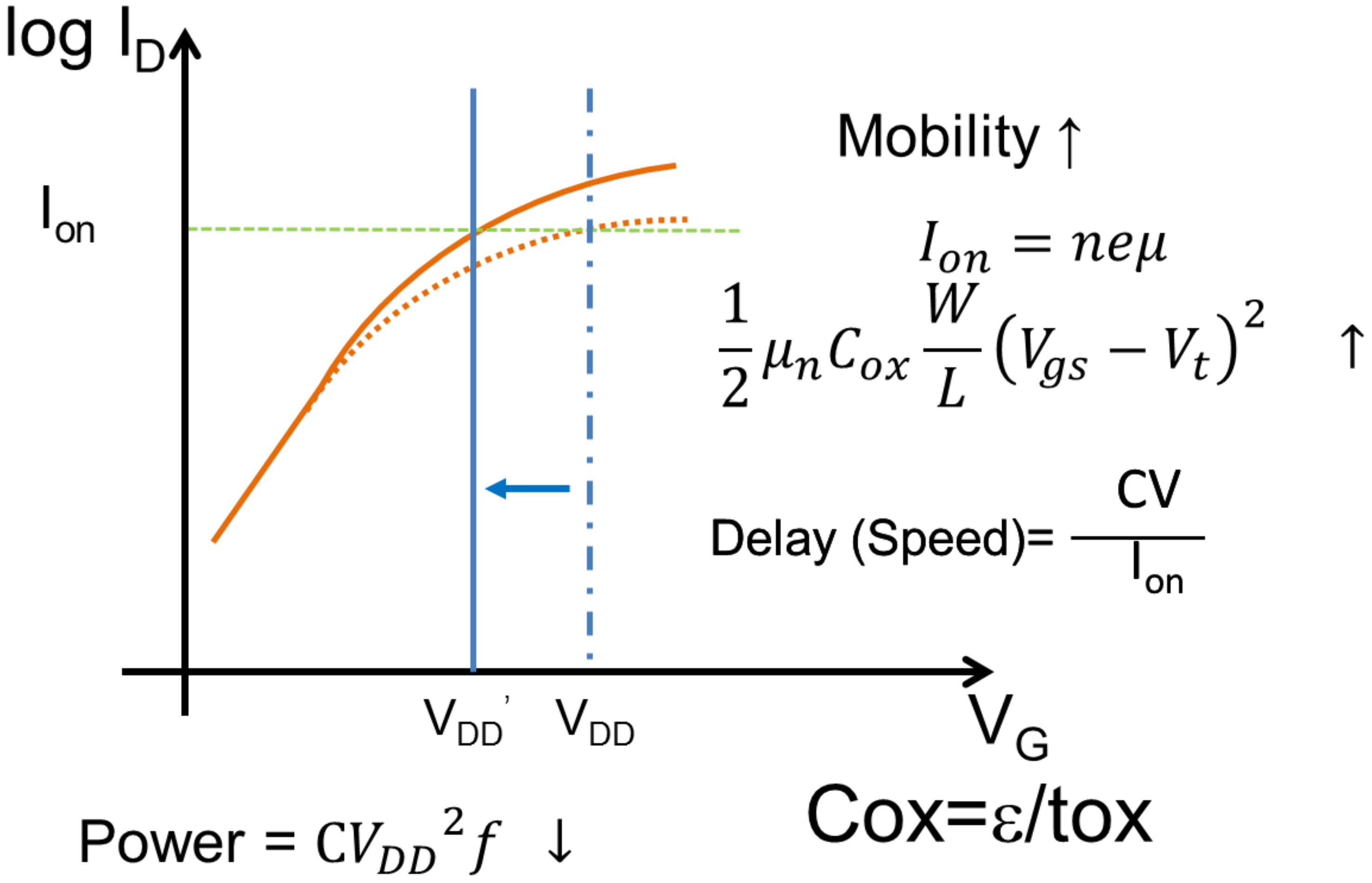
$CV_{DD}{}^2 f$ → small V_{DD} → small SS → FinFET

I_{off} : small tunneling (many sources)

- μ: high mobility, ε: high K, 3D transistor: W

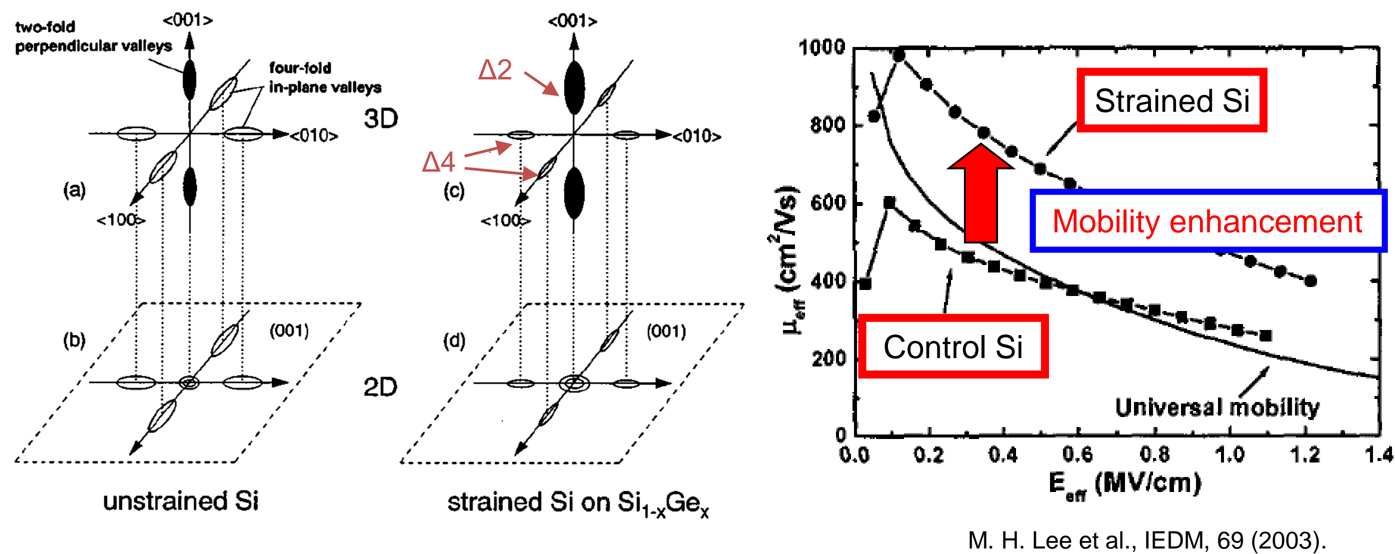

log I_D
I_{on} : large, $\frac{CV}{I_{on}}$
slope: SS small,
small V_{DD} ,
small dynamic
power dissipation CV_{DD}^2f
I_{off} : small
V_{DD}
V_G
$I_{off}V_{DD}$: low leakage power

Power Saving : To Increase Mobility/high K



- Channel: Strained Si => SiGe=> Ge ?

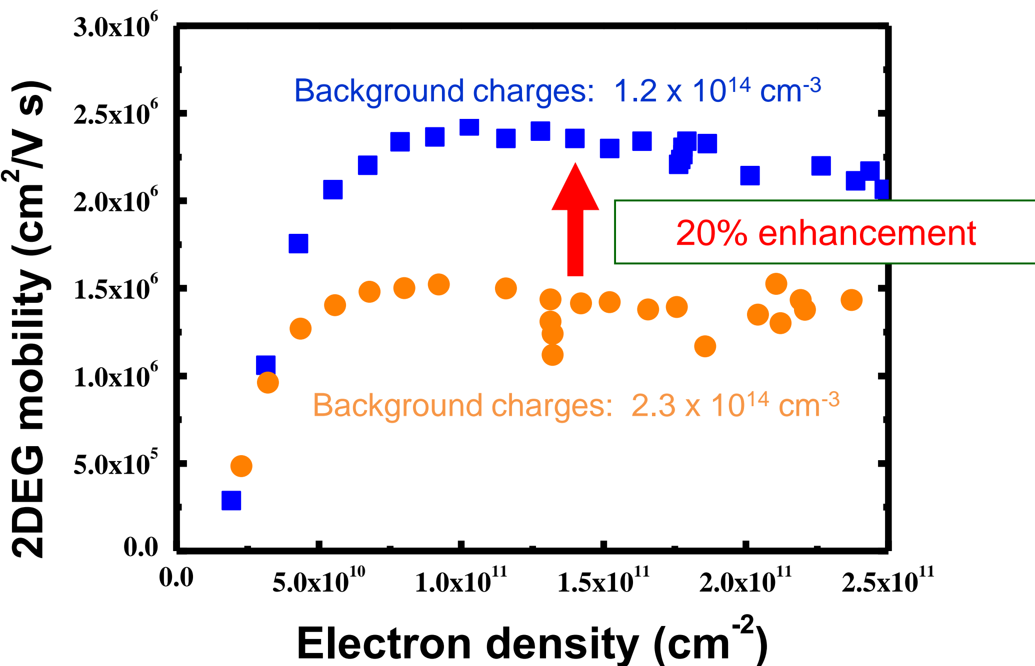
Strained Si at room temperature (90 nm)



M. H. Lee et al., IEDM, 69 (2003).

- The tensile strain lowers Δ2 valleys with low in-plane effective mass.
- More electron in high mobility Δ2 valleys
- ~2x enhancement
- Hole?

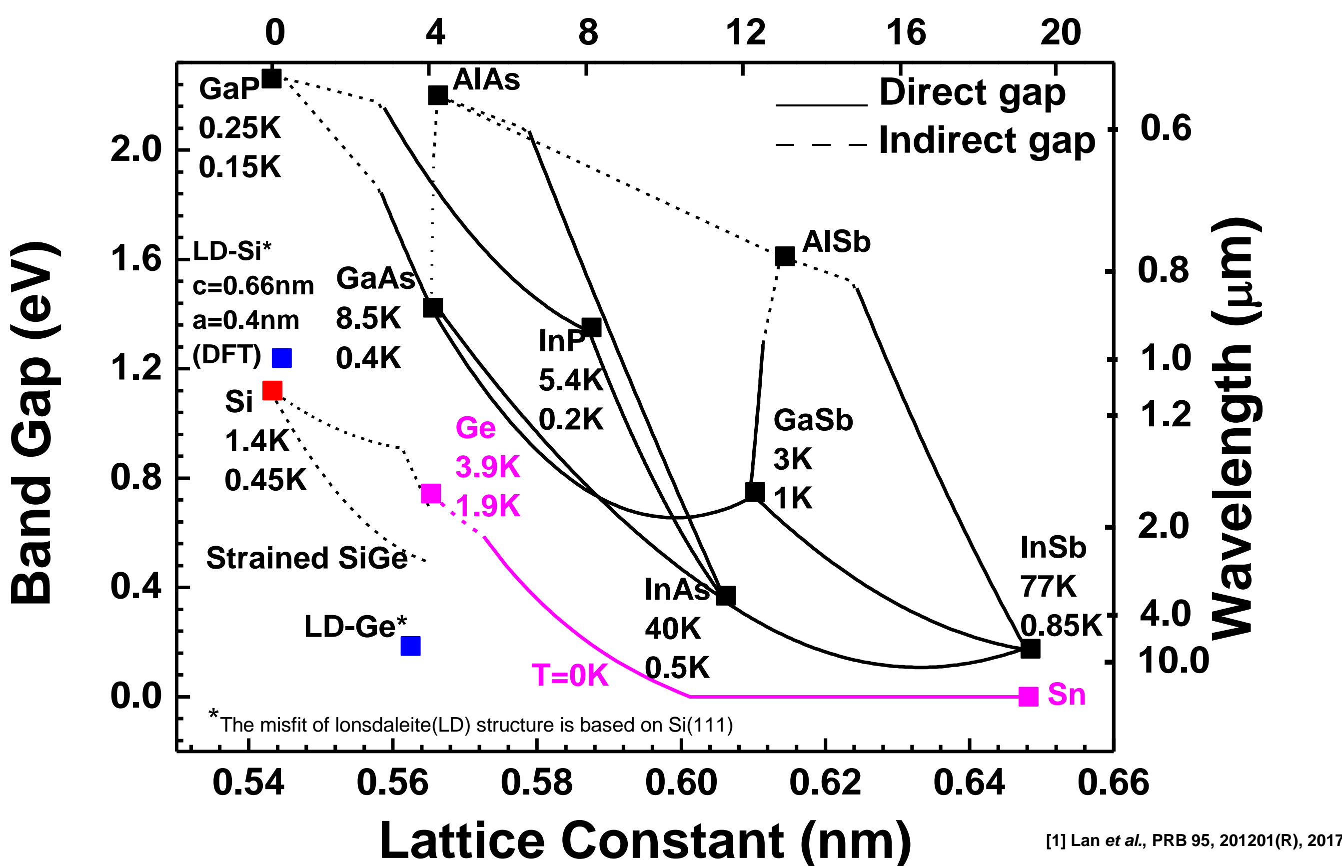
Record High 2DEG Mobility (2.4 M cm^2/V s)



M. Yu. Melnikov et al., APL, 106, 092102 (2015).

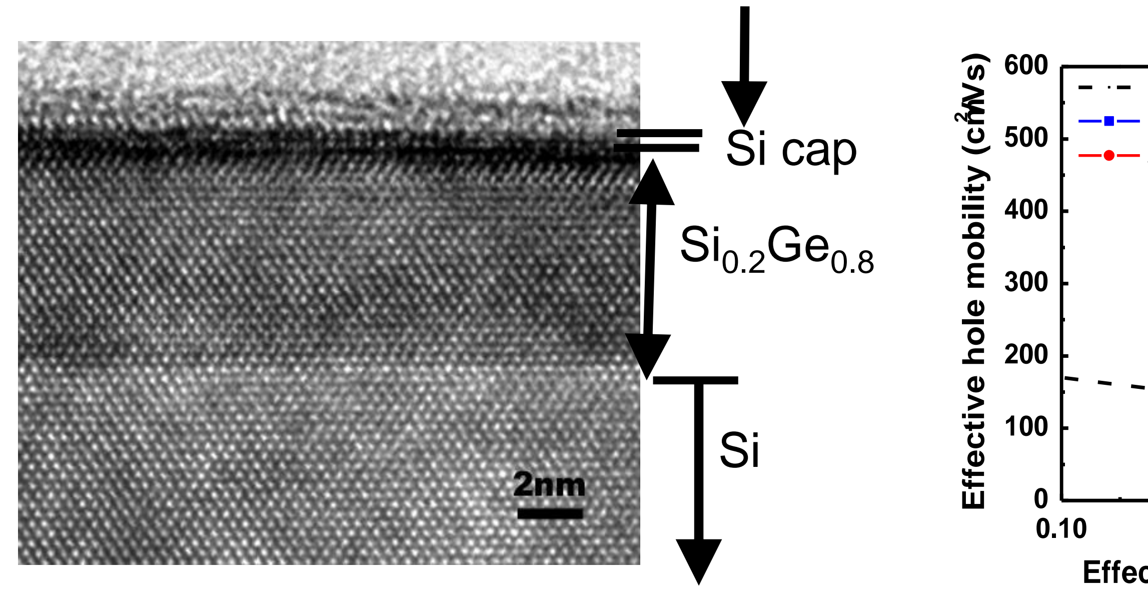
Collaborate with Prof. S. V. Kravchenko, Northeastern Univ.

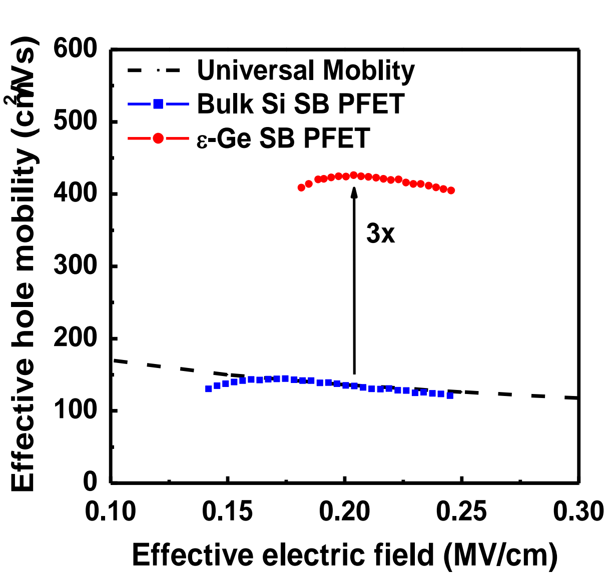
- 2.4 × 10^6 cm^2/V s by the reduction of background charges from 2.3 x 10^{14} cm^{-3} to 1.2 x 10^{14} cm^{-3}.



- **Ge has 3x electron mobility and 4x hole mobility of Si.**

SiGe channel PFET using Si cap

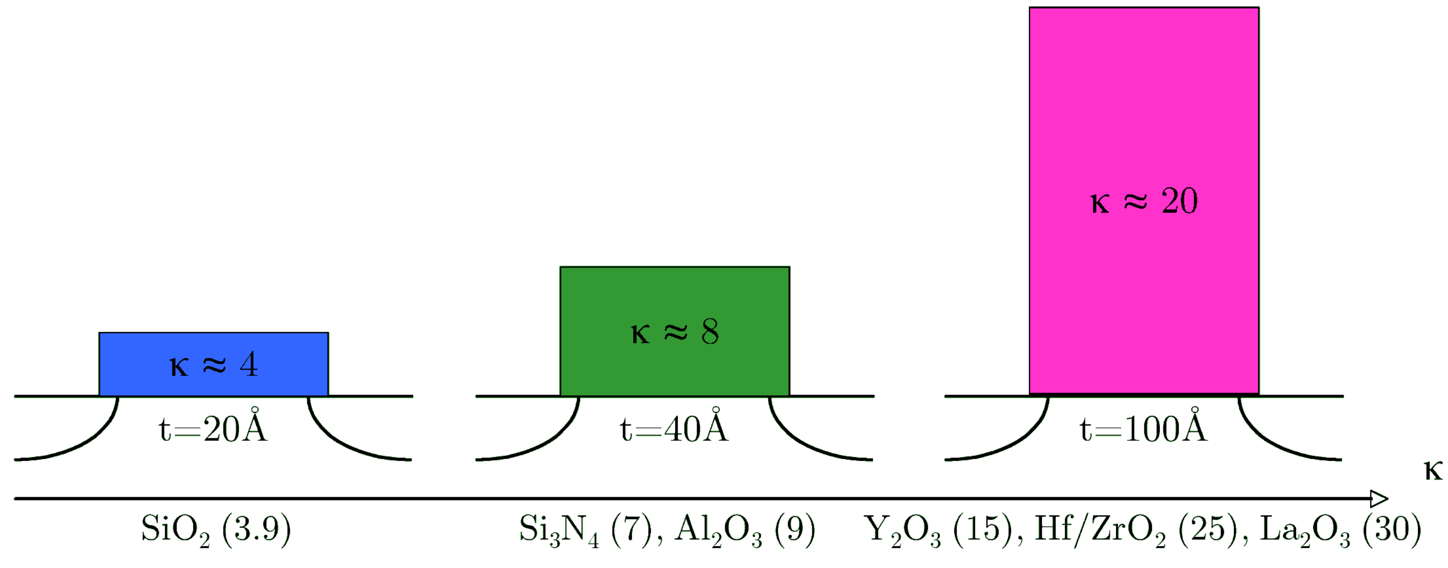




- Si cap for high K/metal gate
- 3x mobility enhancement

C.Y. Peng APL 2007, ROC patent 2006

Effects of High-k



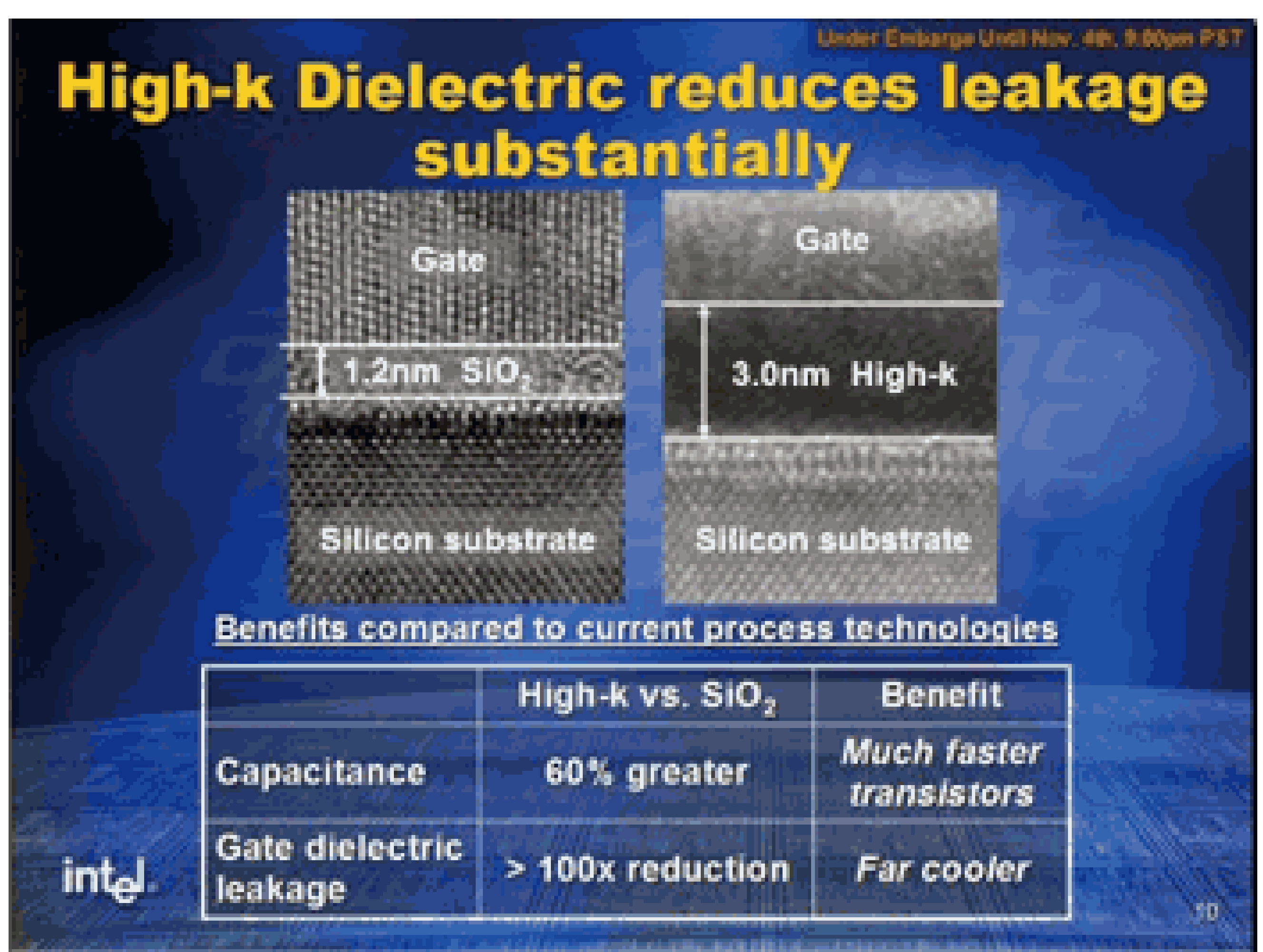
$$I_{on} = \frac{\mu_{eff} C_{ox,\,inv}}{2} \frac{W}{L} (V_{gs} - V_T)^2, \text{ where } C_{ox,\,inv} = \frac{\kappa \varepsilon_0 A}{T_{inv}} \quad (1)$$

High-k

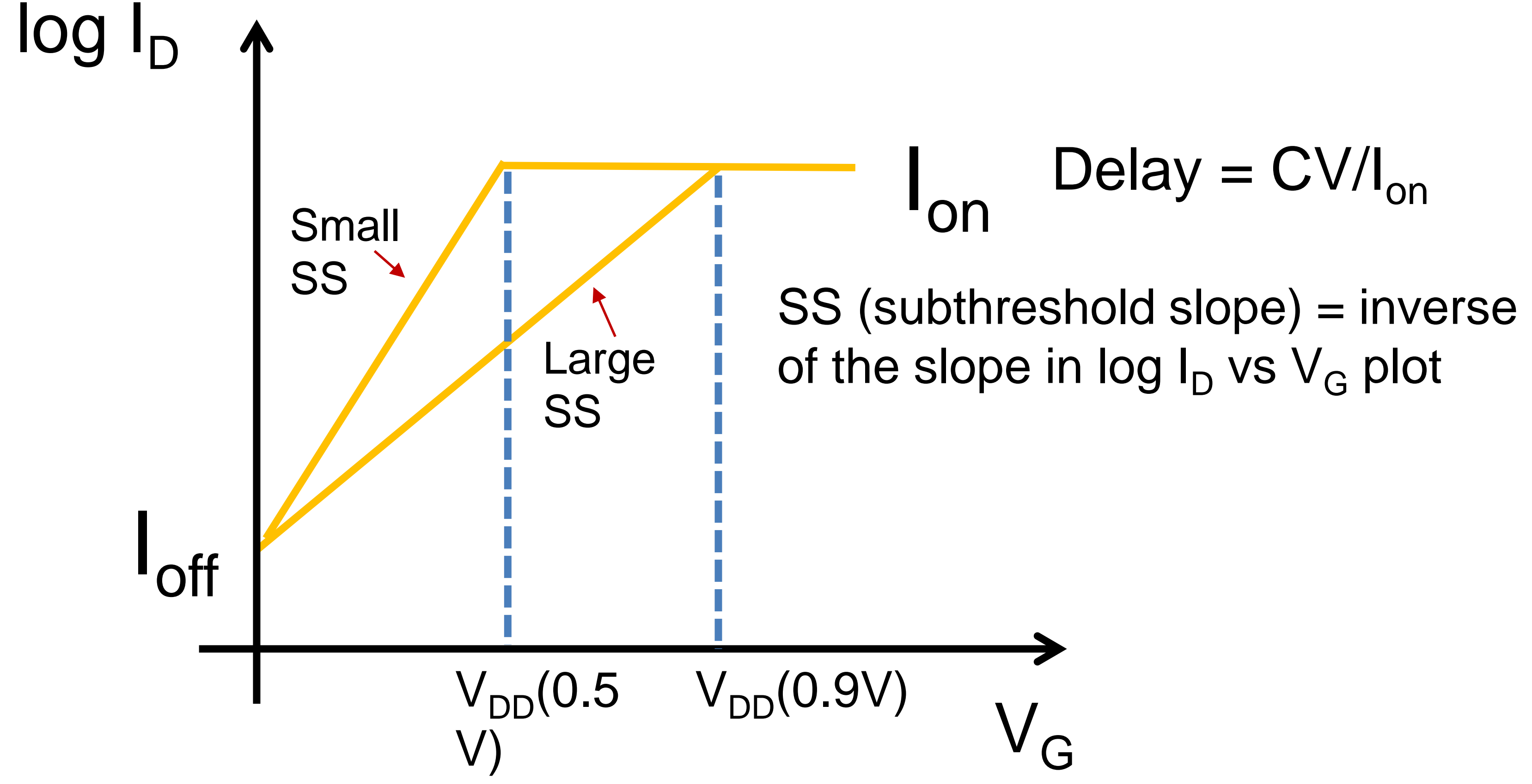
Metal Gate

$$EOT = t_{\text{high-k}} \left(\frac{k_{\text{SiO}_2}}{k_{\text{high-k}}} \right)$$

- k ↑, $C_{ox,\,inv}$ ↑, I_{on} ↑
- k ↑, $t_{high\text{-}k}$ ↑, leakage ↓


High-k Dielectric reduces leakage substantially
Gate
1.2nm SiO2
Silicon substrate
Gate
3.0nm High-k
Silicon substrate
Benefits compared to current process technologies
High-k vs. SiO2
Benefit
Capacitance
60% greater
Much faster transistors
Gate dielectric leakage
> 100x reduction
Far cooler
intel

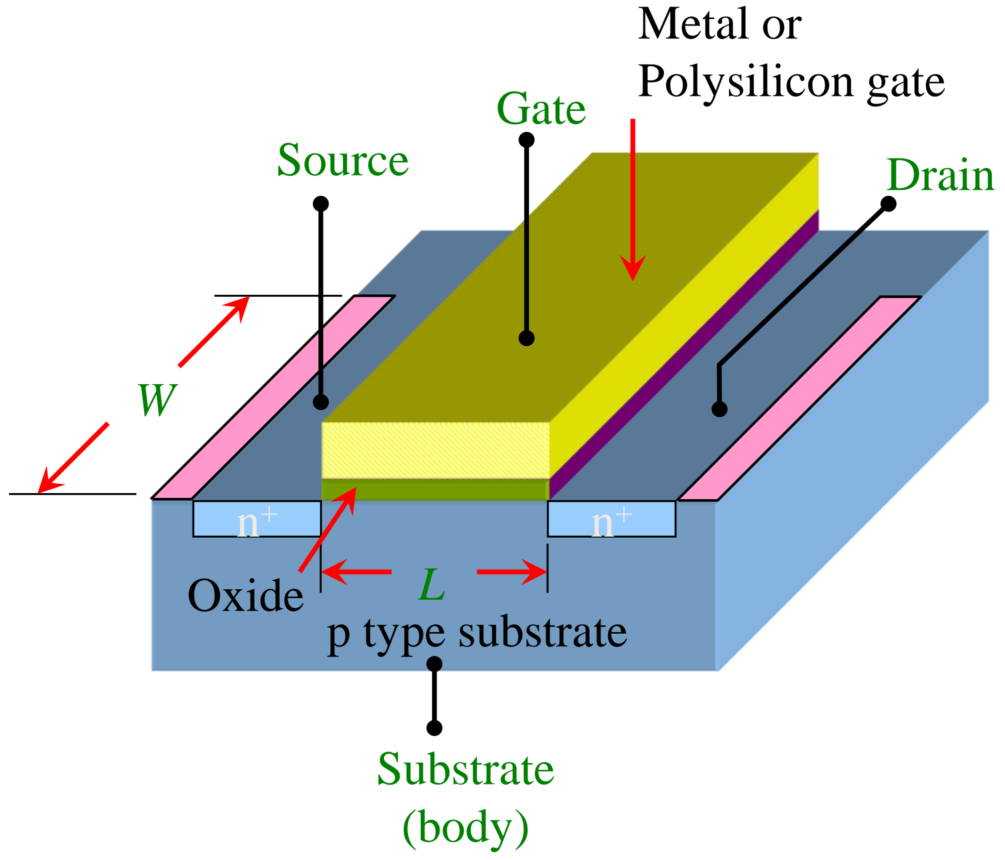
Reduce to Power (= CV_{DD}^2f) by 3D transistor → small V_{DD}



- SS ≥ 60 mV/decade for thermionic emission, 3D transistor
- SS ≤ 60 mV/decade → Steep slope: NCFET , TFET(X)

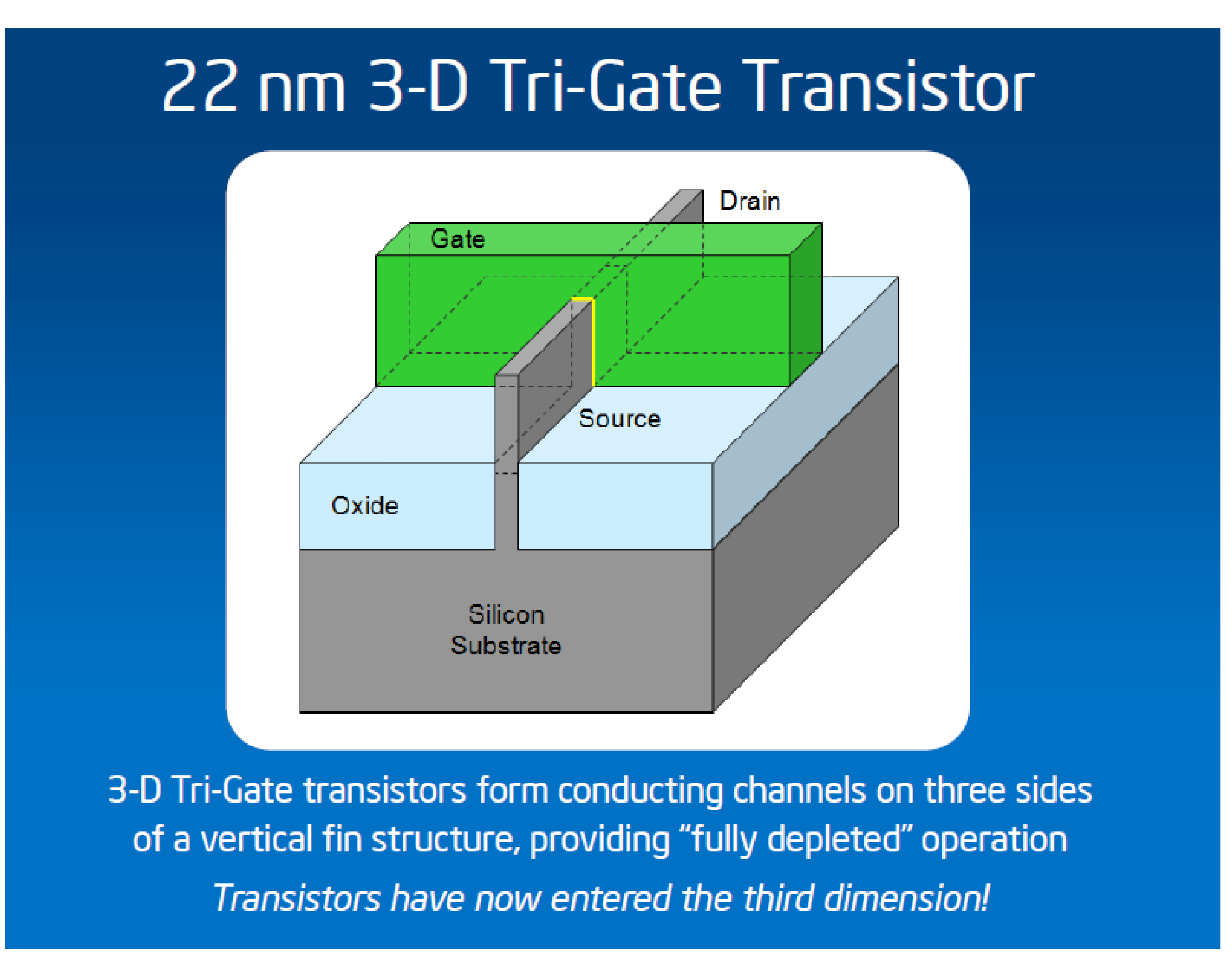
Planar MOSFET structure upto 20/22nm

Smallest dimension?



Historically, L is the technology node up 250 nm/350 nm

FinFET 3D transistors to reduce SS

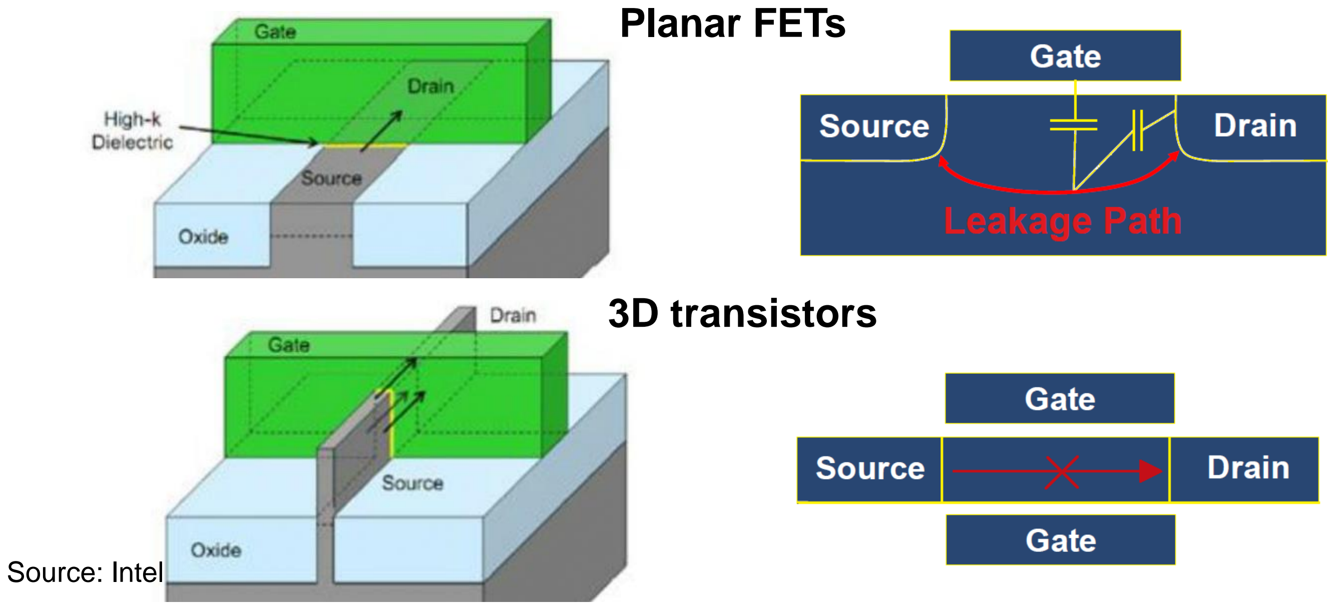


Make your own FinFET

- One piece of paper for each students

- Wfin needs to be small:
  footprint, DIBL (electrostatic)

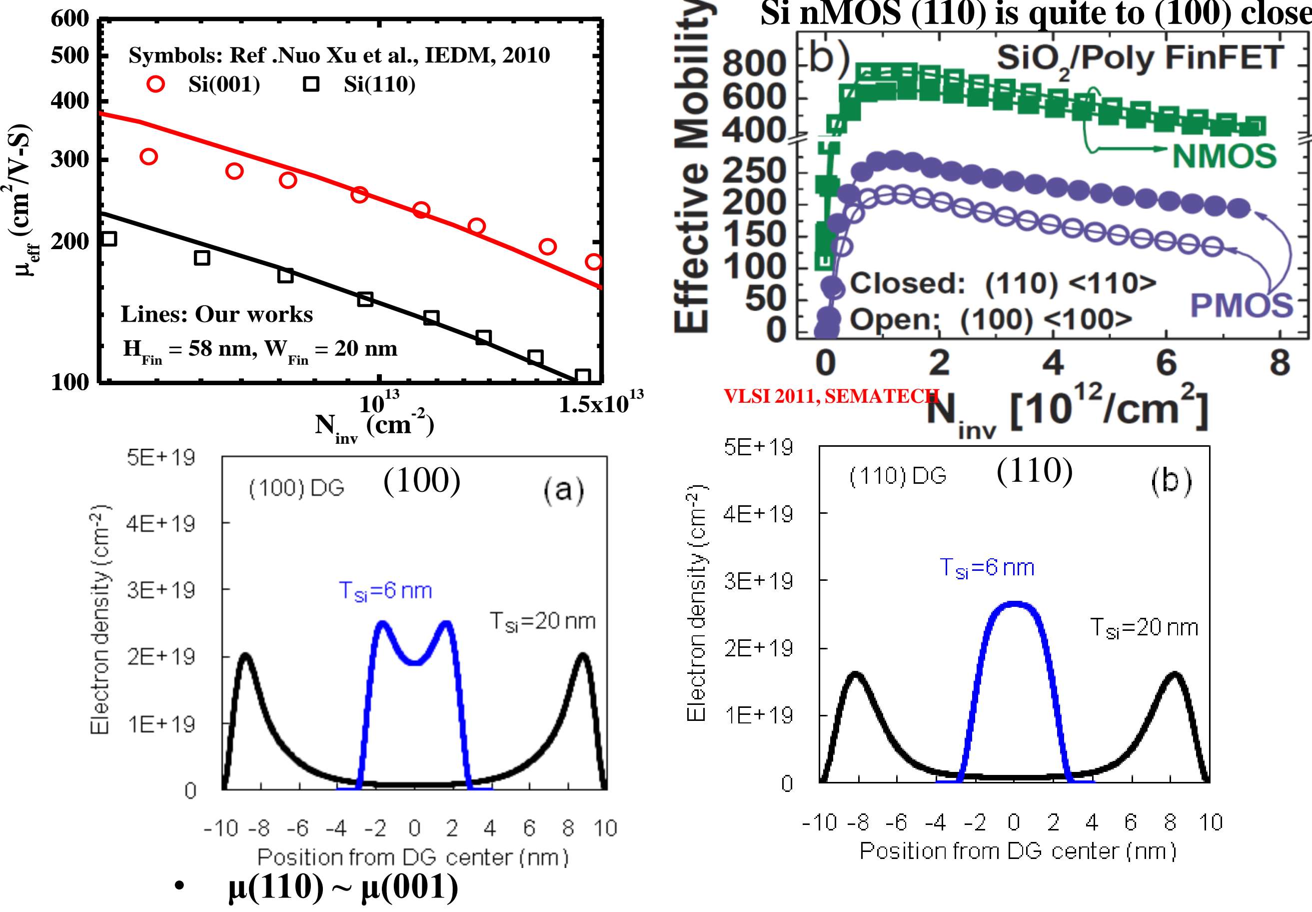
3D Transistors to Reduce SS



Source: Intel

- Current can NOT go through at Vgs=0V.
- SS approaches 60 mV/dec (70 mV in real devices)
- Thinner is better?

ref: C.Hu, "Modern Semicon. Devices for ICs" 2010, Pearson



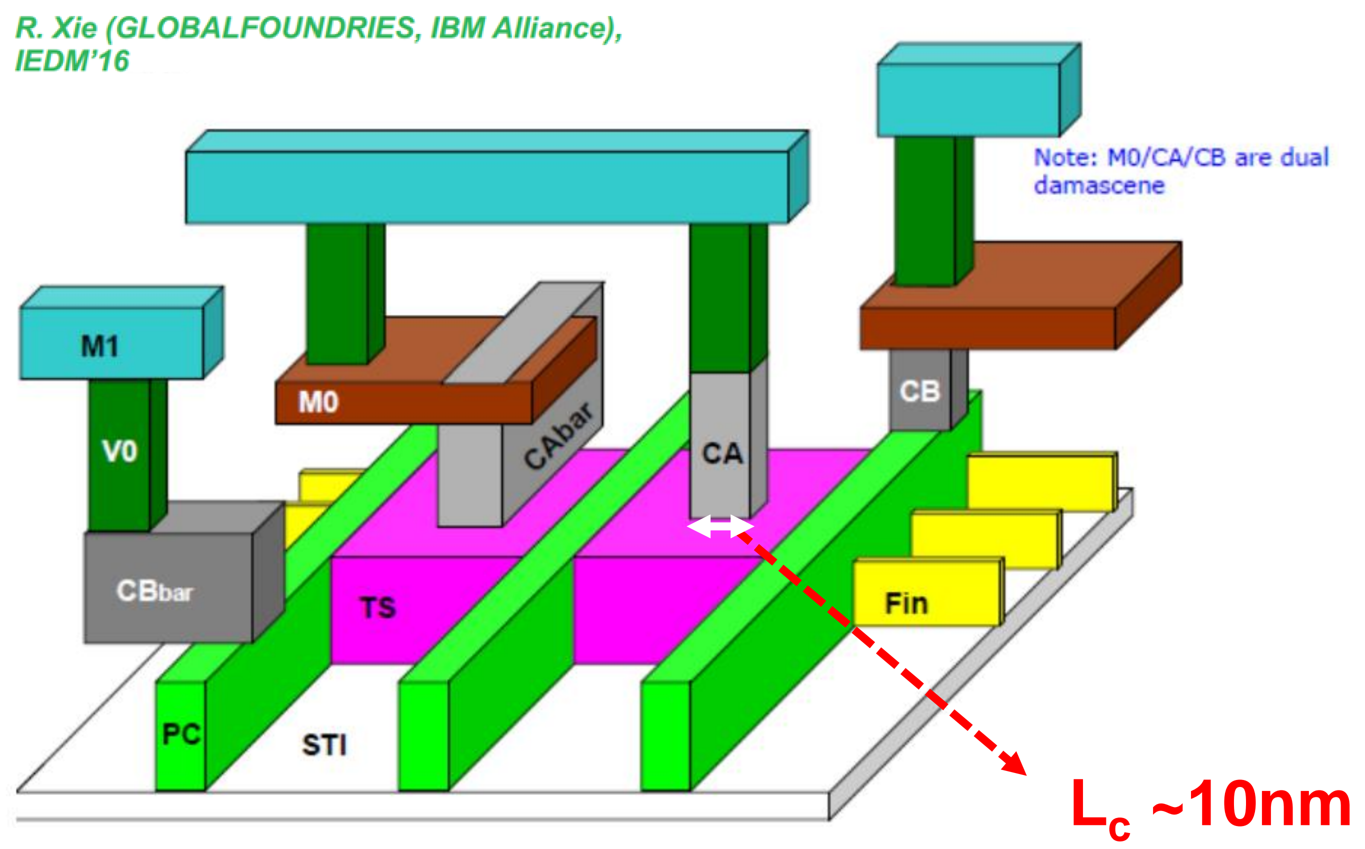
- μ(110) ~ μ(001)
- **Volume Quantization in (110) double gate FET Enhances electron mobility**
- **(110) sidewalls are much easier to reach volume inversion.**

FinFET特性：Intel 22nm (where is 22 nm?)

	Intel (22 nm) [1]	TSMC (16nm)[2]	Intel (14nm)[3]	IBM (14nm)[4]
Fin pitch (nm)	60	48	42	42
Gate pitch (nm)	90	90	70	80
Fin height (nm)	38		42	
On current (uA/um)	@Vdd=0.8 Ioff=10nA PMOS: 950 NMOS: 1070	@Vdd=0.75 PMOS:960 NMOS: 925	@Vdd=0.7 PMOS: 1040 NMOS: 1040	@Vdd=0.8 PMOS: 935 NMOS: 808
DIBL(mV/V)	PMOS: 50 NMOS: 46	<40	PMOS: ~60 NMOS: ~75	~40
S.S. (mV/dec)	PMOS: 72 NMOS: 69	<70	~65	PMOS: 71 NMOS: 67

- **Intel has the largest on current than others.**
- **Intel use self-aligned double patterning(SADP) to form minimum interconnects pitch of 52nm (M2).**

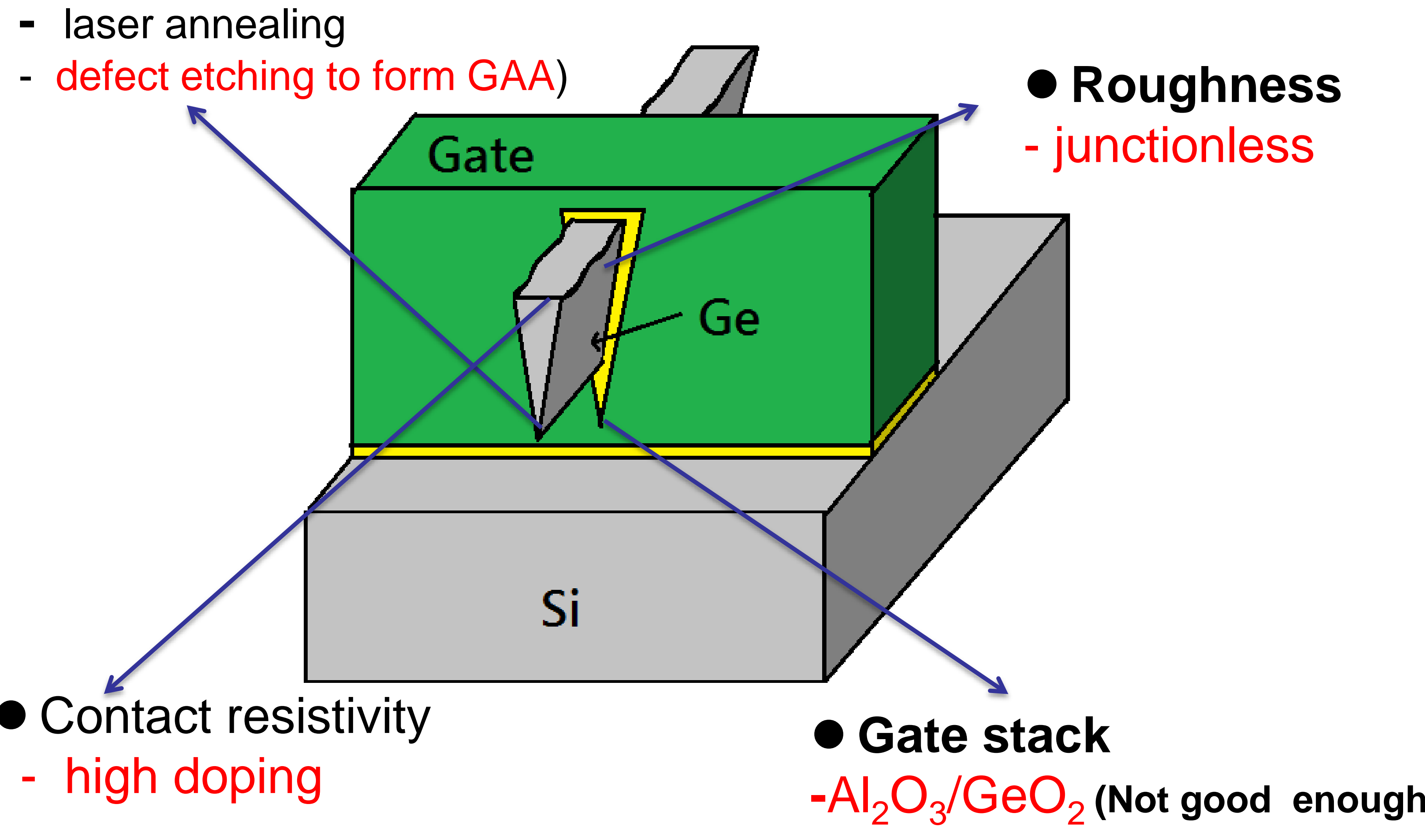
Ref[1]:Auth, Chris, et al. VLSI 2012
Ref[2 : IEDM 2013
Ref[3]: S. Natarajan , et al. IEDM 2014
Ref[4]: C-H. Lin , et al. IEDM 2014



Fin Pitch, Gate Pitch, Fin Height, Fin Width

Beyond FinFET: Gate All Around

- **Defect control**



Beyond FinFET: stacked GAA

- Epi

-strain engineering: fully compressive strain for stacked GeSn channels

-defect and dislocation: defect confinement at Ge/SOI interface

-inter-channel uniformity: sacrificial layers design

- Channel release

-etching selectivity: H_2O_2 etching

-Inter-channel uniformity & line edge roughness: sacrificial layers etching with ultrasonic assist technique

-effective mass & strain after channel release: biaxial to uniaxial strain & microbridge effect

Gate

Oxide

Si

- Low thermal budget gate stacks

-low D_{it} of IL, high-k material, and low dispersion: $TiN/ZrO_2/Al_2O_3$+RTO with 400°C thermal budget

- S/D:

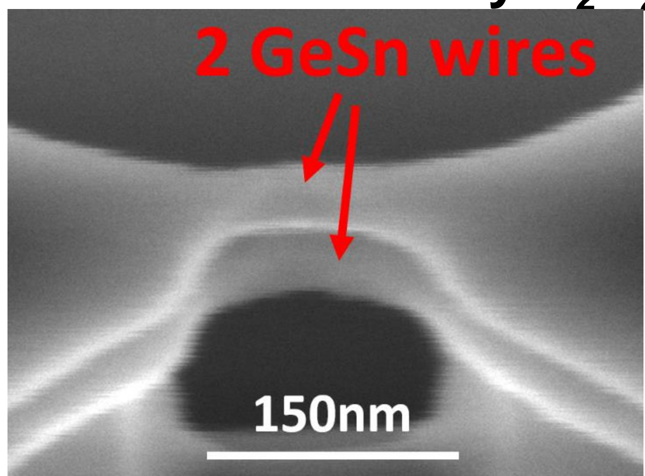
-high doping

-low parasitic resistance

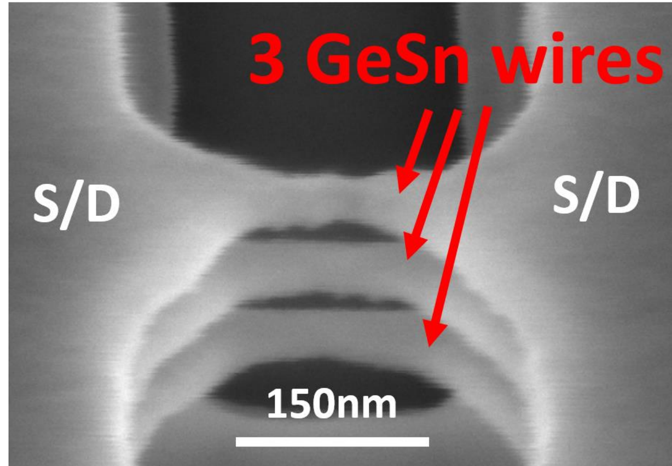
➔ Optimization for *in-situ* doped GeSn S/D and PtGeSn/PtGe formation to decrease parasitic resistance are achieved.

Solution to stacked channel

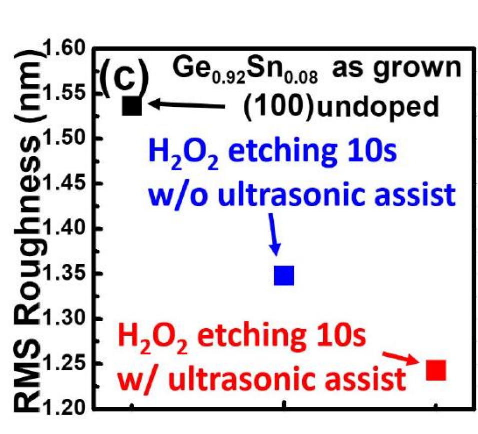
Channel release by H_2O_2 etching



Tilt 52°

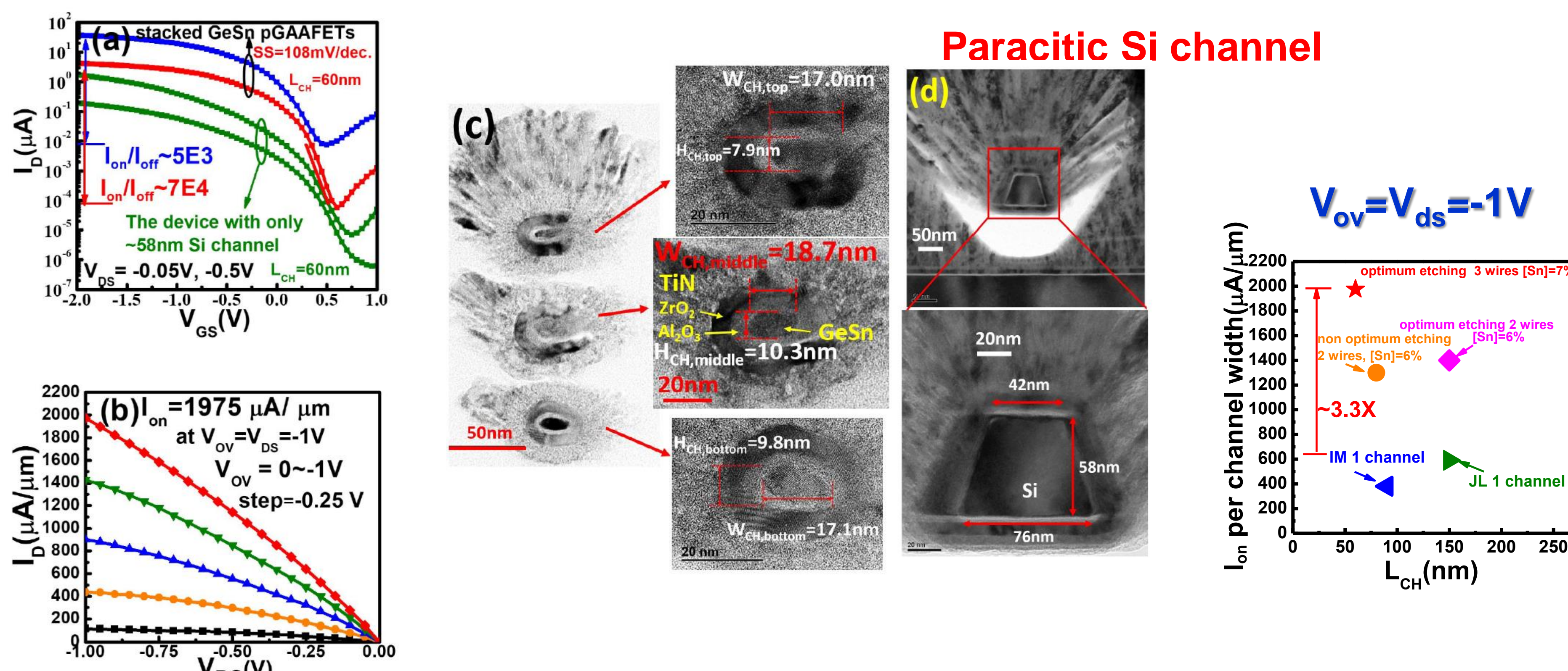


Tilt 52°



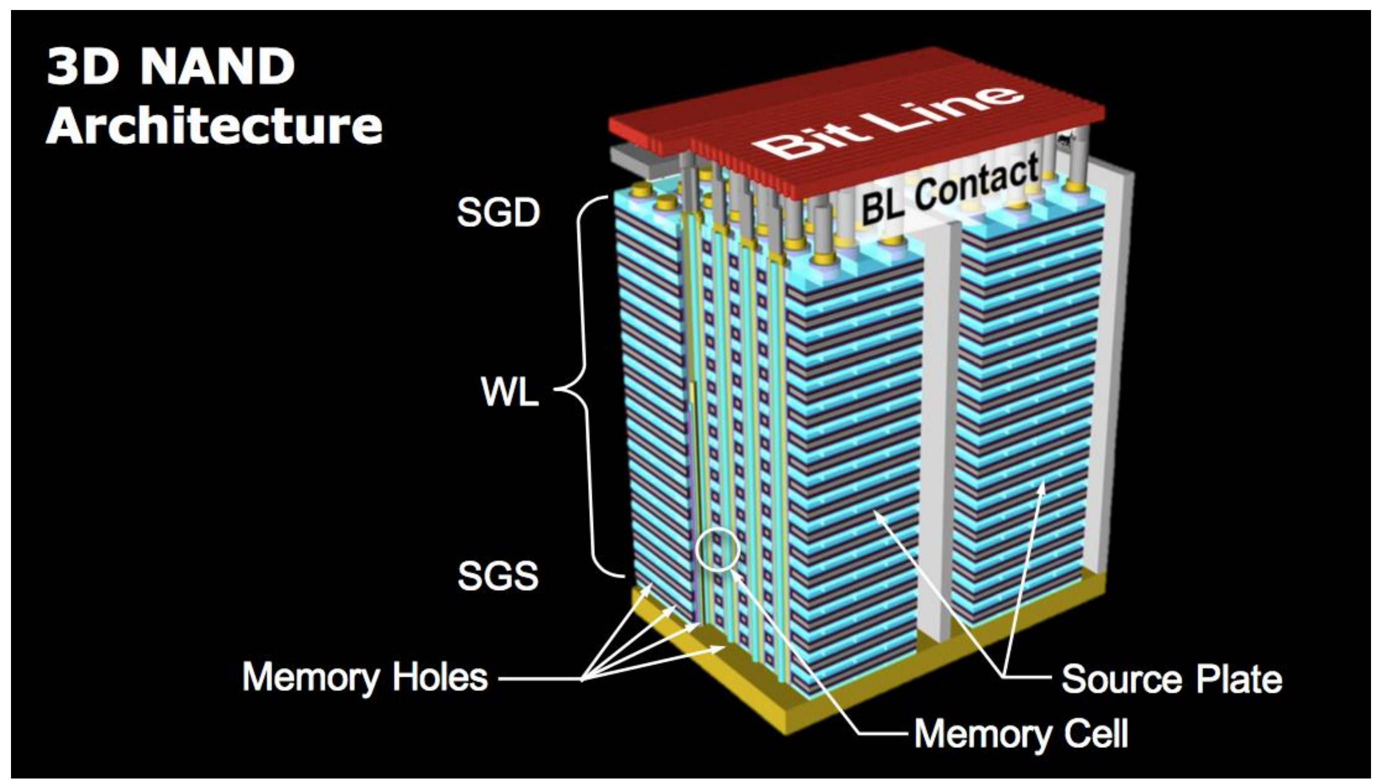
- **Pure Cl_2 or HBr anisotropic etching to form the fin-structure.**
- **H_2O_2 wet etching further removes the Ge sacrifacial layer to form stacked GeSn wires.**
- **SnO_x remains on GeSn surface to achieve high etching selectivity.**

Stacked 3 channels $Ge_{0.93}Sn_{0.07}$ JL pGAAFETs with optimum ultrasonic-assisted H_2O_2 process



- I_{on}=1975μA/μm at V_{OV}=V_{DS}=-1V with 3 channels.
- Si parasitic channels has much smaller I_{on} and due to large ΔEv at Ge/Si, parasitic resistance for un-intentionally doped Ge and lightly doped Si.

3D NAND Flash

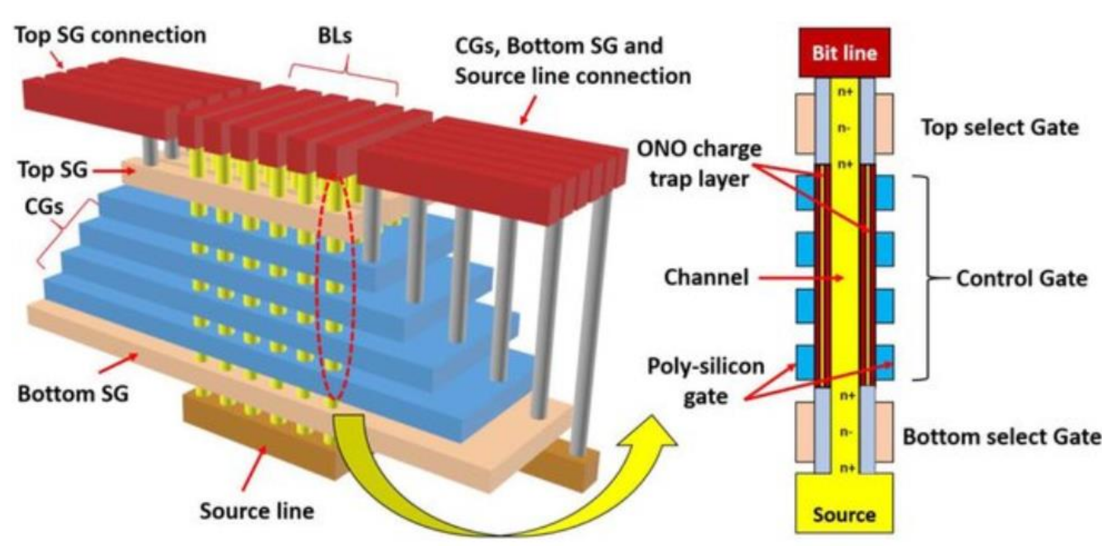


SGD: select gate at the drain end
SGS: select gate at the source end

Source: Western Digital, DevelopEX 2017

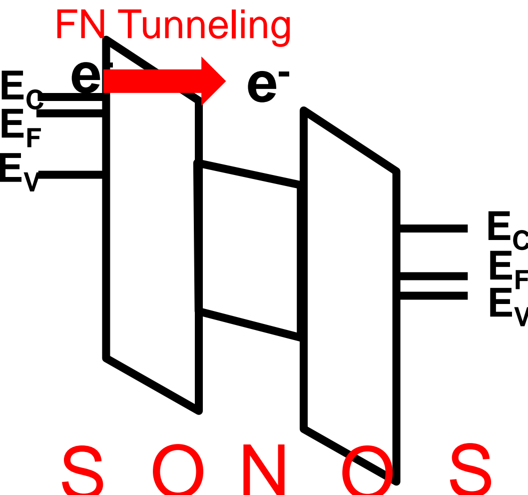
3D NAND (96, 128 L)

- **3D NAND Flash structure**



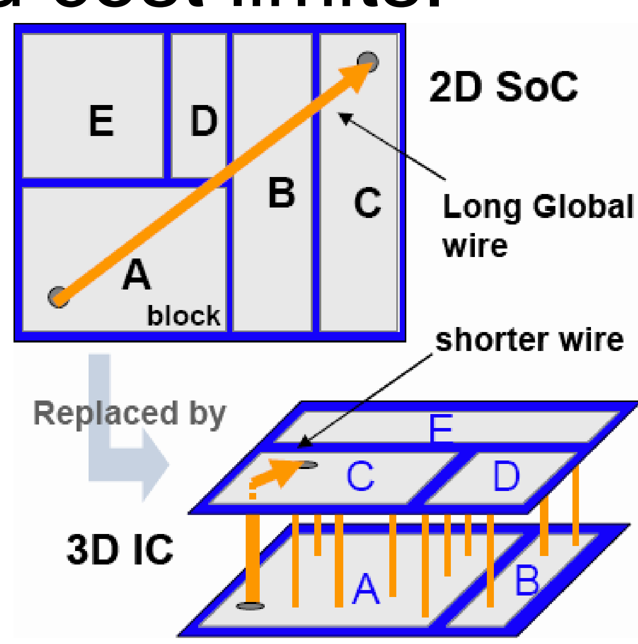
- **Structure**
  - **SONOS**

Silicon-Oxide-Nitride-Oxide-Silicon



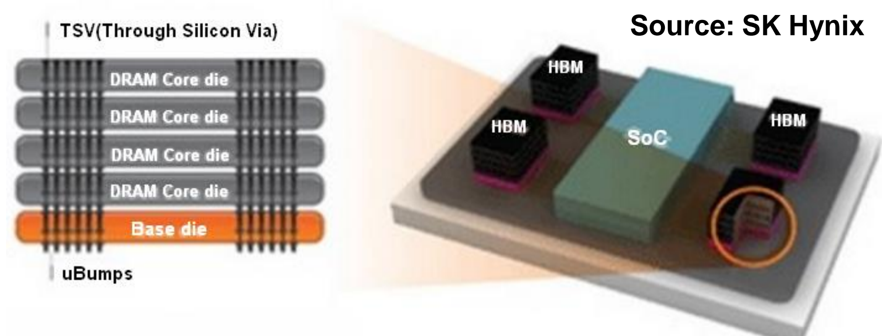
3D IC

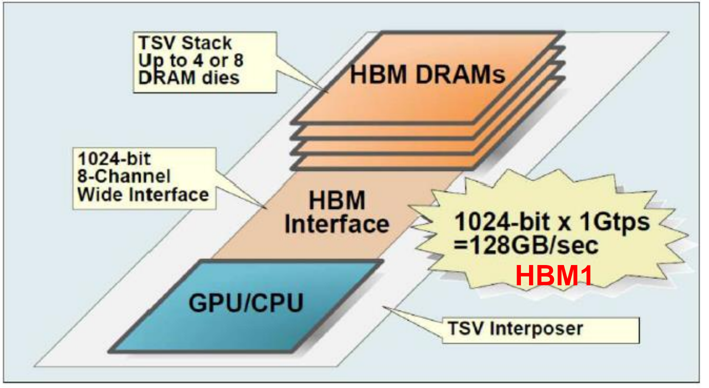
- Scaling faces physical and cost limits.
- Size reduction
- High interconnect density
  - Faster
  - Less power consumption
- Hetero-integration
  - Memory, logic, optical, MEMS, RF chip



TSMC course

High Bandwidth Memory





(256GB/sec for HBM2)

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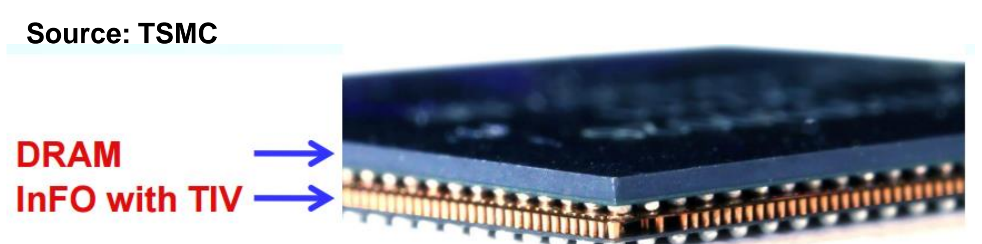
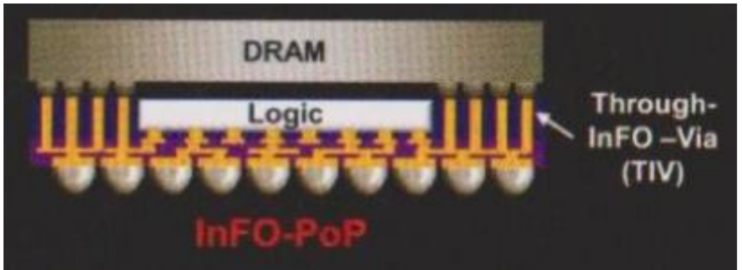
- Stacked DRAM dies, connected by TSVs
- Size reduction, but high density

DRAM on Application Processor

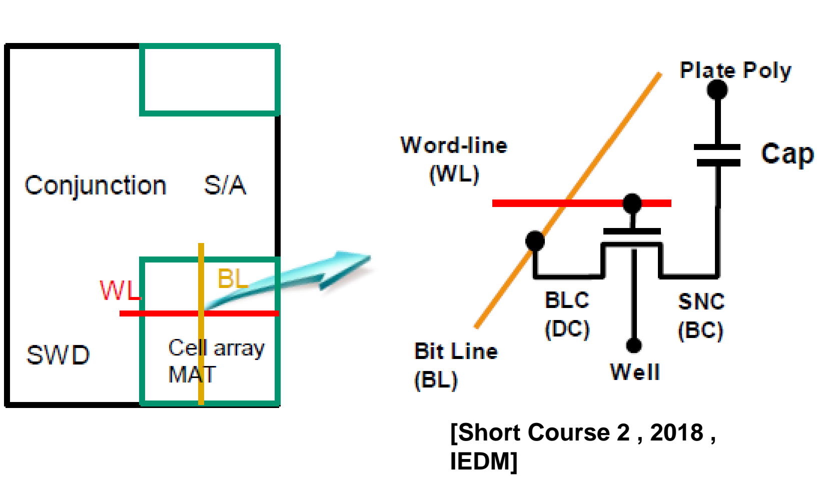
Source: TSMC



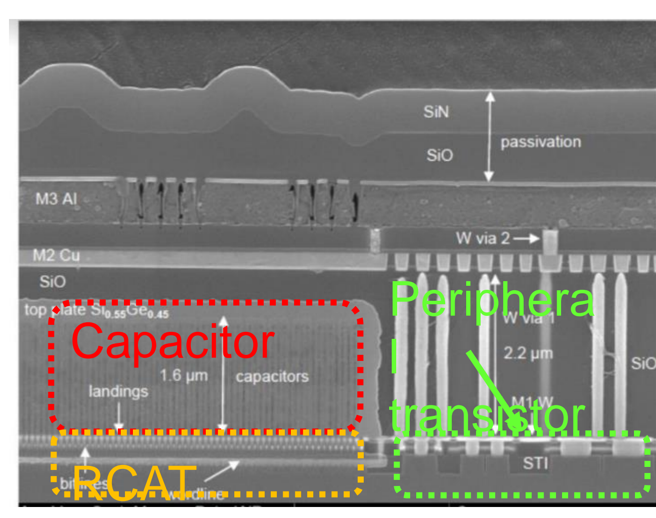


- Vertical interconnects in molding compound (TIV)
- Stacked DRAM dies on application processor (AP)
- No additional substrate → Low cost

DRAM Architecture



[Short Course 2 , 2018 , IEDM]

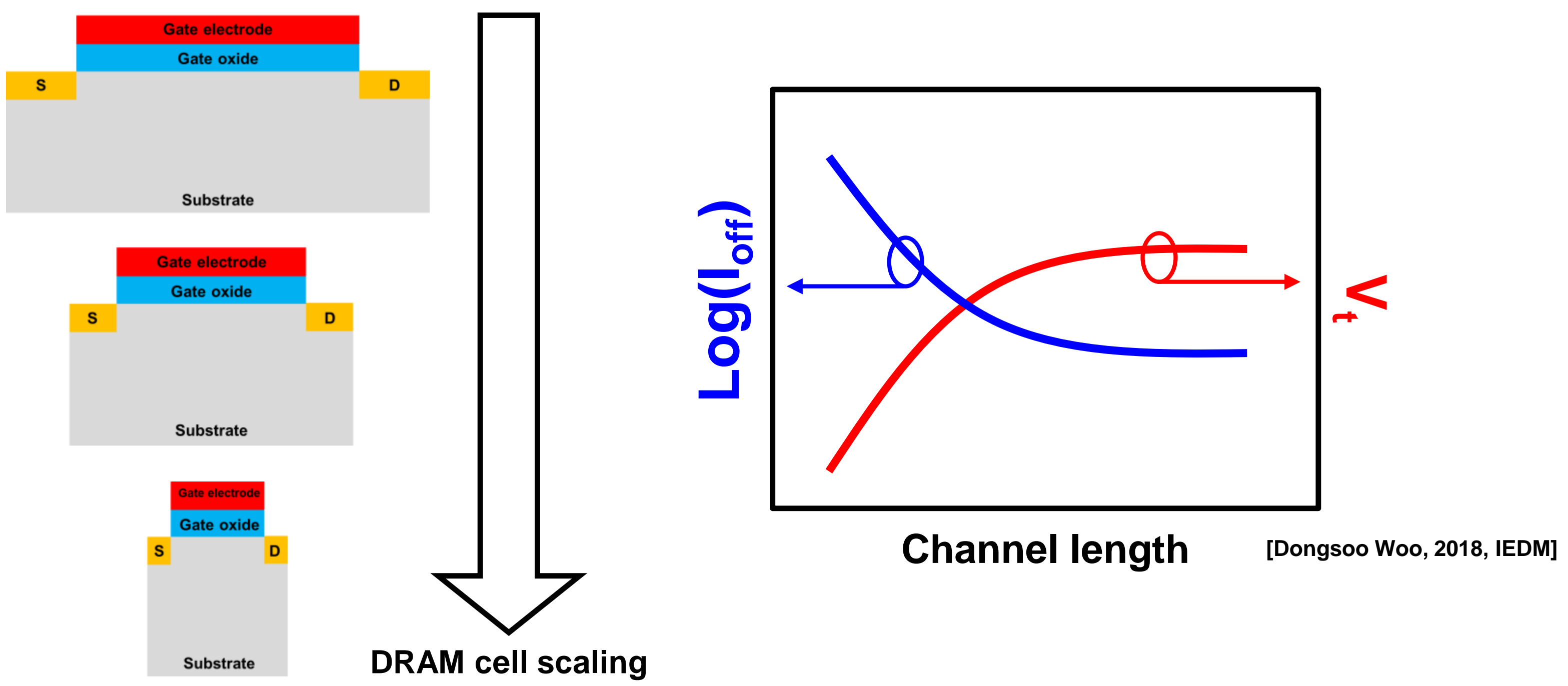


Samsung 26nm 4Gb DRAM cross-section (source: Chipworks)

- **DRAM consists of**
  - **1. RCAT (Recessed Channel Array Transistor)**
  - **2. Capacitor**
  - **3. Peripheral transistor (regular logic transistor)**

1T/1C

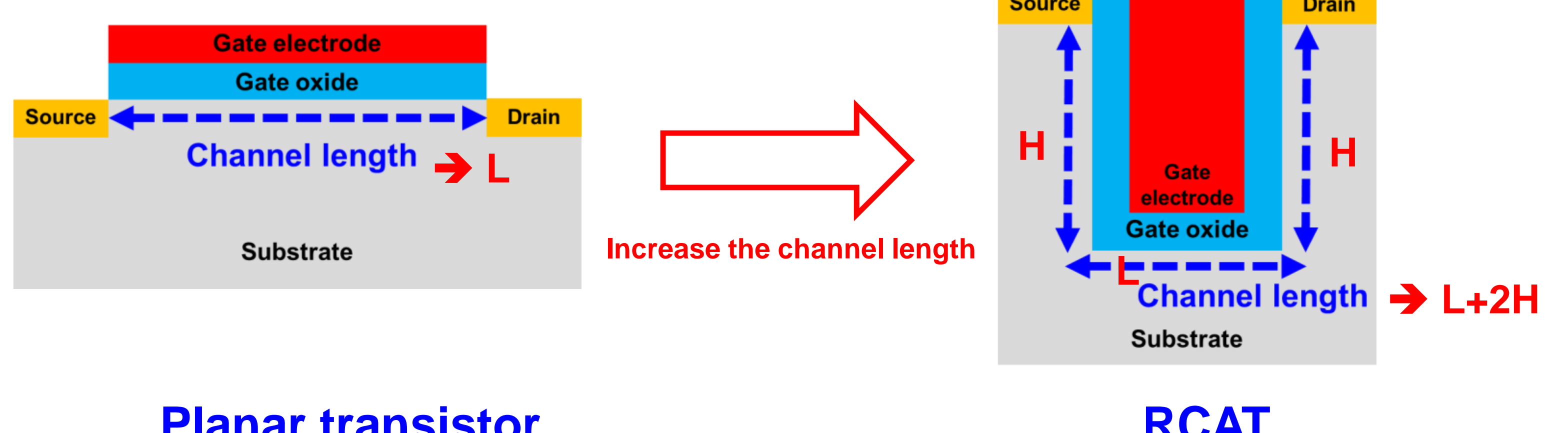
RCAT



- **Retention time ➔ 64 ms (JEDEC Spec.) ➔ need low leakage current (1fA/cell)[1]**
- **DRAM cell scaling ➔ short channel effect**
- **DRAM cell transistor should be long channel to reduce the off current.**

[1] [Kinam Kim, 2007, IEDM]

RCAT



Planar transistor

RCAT

- **Channel length of transistor increases by recessed channel to prevent short channel effect.**
  - **Planar transistor ➔ 1-dimensional channel**
  - **RCAT(Recessed channel Access Transistor) ➔ 2-dimensional channel**
  - **Channel length: RCAT (L+2H) > Planar transistor L**

Emerging memory

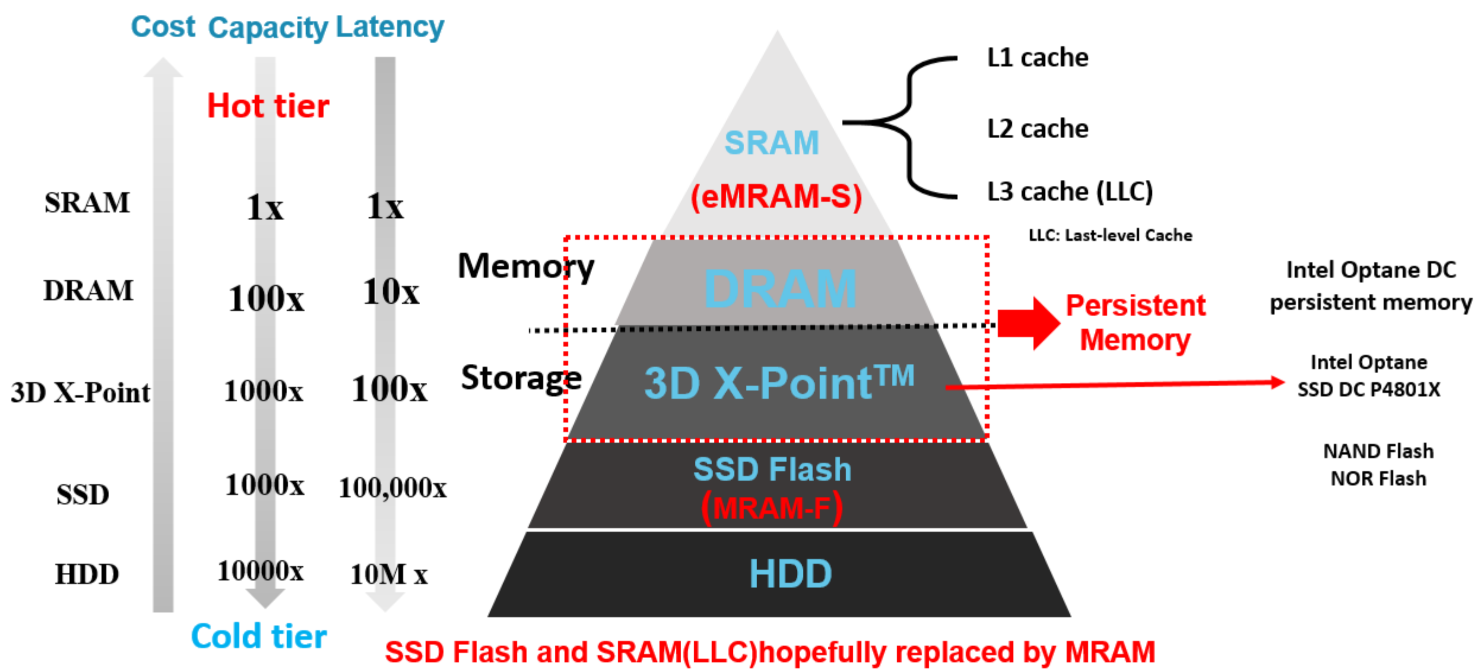
(source: IEEE Solid State circuit Mag.) Col.8 no.43, 2016))

TABLE 1. DEVICE CHARACTERISTICS OF MAINSTREAM AND EMERGING MEMORY TECHNOLOGIES.

	MAINSTREAM MEMORIES				EMERGING MEMORIES		
			FLASH				
	SRAM	DRAM	NOR	NAND	STT-MRAM	PCRAM	RRAM
Cell area	>100 F^2	6 F^2	10 F^2	<4F^2 (3D)	6~50F^2	4~30F^2	4~12F^2
Multibit	1	1	2	3	1	2	2
Voltage	<1 V	<1 V	>10 V	>10 V	<1.5 V	<3 V	<3 V
Read time	~1 ns	~10 ns	~50 ns	~10 μs	<10 ns	<10 ns	<10 ns
Write time	~1 ns	~10 ns	10 μs–1 ms	100 μs–1 ms	<10 ns	~50 ns	<10 ns
Retention	N/A	~64 ms	>10 y	>10 y	>10 y	>10 y	>10 y
Endurance	>1E16	>1E16	>1E5	>1E4	>1E15	>1E9	>1E6~1E12
Write energy (J/bit)	~fJ	~10fJ	~100pJ	~10fJ	~0.1pJ	~10pJ	~0.1 pJ

Notes: F: feature size of the lithography. The energy estimation is on the cell-level (not on the array-level). PCRAM and RRAM can achieve less than 4F^2 through 3D integration. The numbers of this table are representative (not the best or the worst cases).

Memory hierarchy



- **To meet the high performance (high capacity, low latency , low power) → persistent memory, MRAM**

Ref: 2017, IEDM, Short Course2

How much can you know

1. SiGe 的好處，至少一項
2. What is USB memory？ DRAM, FLASH, SRAM?
3 What is the PPACR?
4. FinFET 和平面電晶體之不同為何？
5. 寫出4種使Ion變大的方法。
6. 為什麼Ion要大?
7. 寫出2種使Vdd變小的方法。

.

8.為什麼Vdd要小?

9. 理論上 5nm node 的電晶體面積是7nm node 的幾倍？

10. 10nm node 的下一代是幾奈米？

11.18吋晶圓的面積是12吋晶圓的幾倍?

12. APPLE A10 的 用FinFET or Planar transistor

13.What is the access transistor of DRAM?

14.How many layers of 3D NAND?

15.What are memory gaps in memory Hierarchy？

Summary

- Broad applications: A, B, C
- Smart phone is still the killer application
- New technologies (7,5, 3 nm) for computing
- Old technologies + background knowledge for More than Moore.
- MEMORY is the key to success